Document Number: MPC8572DS
Rev. 2.1, 4/2008

MPC8572DS (Whitefin) Development System Errata

1 Overview

This document describes the known errata and limitations of the Whitefin Development System. In all cases, if an errata has a work-around, it is applied to the system before shipped to customers.

The board assembly revision (denoted with a 700 number) is updated every time a new problem or system upgrade is found and systems have been shipped. Pre-production revs are “X1, X2, X3”... and so on. Once in production, valid assembly revs are “A, B, C”... and so on. If your current board revision is rev “B’”, then it has all rev “B” fixes along with all the rev A, as well as all the previous pre-production fixes. A rev “B” board would not have any of the rev “C” fixes.

Regarding the published schematics, the schematic history section found on sheet #2 of the schematics also denotes which errata have been incorporate into the schematic. If no history is present, then no errata has yet been incorporated into the schematic. In such cases, the errata should be applied to the published schematics to determine the correct wiring of the Whitefin system (i.e. after the changes are applied).

Errata are classified into three categories: correctable (CE), uncorrectable (UE), and enhancement requests (ER). The last two categories are not corrected initially, but may be rolled into possible future revisions of the system (if any). Table 1 includes all corrected CE for applicable pre/production systems. Also included are corrected UE and ER for applicable revisions that incorporated them. Schem Rev denotes which revision of the schematic includes these corrections. Table 2 includes all UE and ER that have not been incorporated in any revision to date.

2 CORRECTED ERRATA or ENHANCEMENT REQUESTS

Table 1. MPC8572DS (Whitefin) Corrected Errata/Enhancement Requests

#	Error/ Type	Problem/Request	Errata Correction		Assy Rev	Schem Rev
			Work-around	Re-spin Resolution		
1	CE1	Need to activate RSMRST circuit that is currently unstuffed so to obtain a properly timed latched emode switch.	De-populate R970 De-populate C913, Populate R958 as 0 ohm. (ALL three located bottom lower left near board edge.)	Same	X2	C.0
2	CE2	ICT or flying probe cannot access vias under key BGAs. This greatly lowers test coverage. Solder mask needs removal from these areas	Corrected by Fab.	Same	X2	NA
3	CE3	R321 and R318 are used to allow SC457 sense circuit to operate without a processor	Replace R321 with 100 ohm resistor. Replace R318 with 100 ohm resistor. Both locate bottom side, upper middle right (just above U57. U57 is tiny chip just above processor.	Same	X2	C.0
4	CE4	Too reduced voltage for Phy clocks (U5) both U17 DUT and U30 Vitesse Phy.	Replace R2 with 47 ohm resistor. It is located top between the two Ethernet connectors J7 and J8. Replace R361 with 47 ohm resistor. It is located bottom side near U17.	Same	X2	C.0

Table 1. MPC8572DS (Whitefin) Corrected Errata/Enhancement Requests

#	Error/ Type	Problem/Request	Errata Correction		Assy Rev	Schem Rev
			Work-around	Re-spin Resolution		
5	CE5	Vcore output capacitors have incorrect type. Currently using too high of ESR value Tantalum capacitors. Need to use low ESR Panasonic.	Replace C94, C115, C124, C90 with Kemet T530D337M004ATE006 (Agile #150-75305) All are on top side around U17 Processor. C99, C91 remain unstuffed.	Same	X2	C.0
6	CE6	These resistors need to be stuffed when NOT using an Interposer, but with 8572 silicon.	Populate R302 and R392 with 4.7K resistors.	Same	X2	C.0
7	CE7	Several Capacitors are not rated with high enough voltage values.	Replace C31, C35, C48, C811, C902 with Agile number 150-30274 which is 100uF 20V (Kemet T491X107M020AT) type capacitors.Remove C37 and C28 33uF capacitors.	Same	X3	C.0
8	CE8	Too much current ripple measured by U57 current mirror. Need to add a 4700pf capacitor in parallel to R329 to filter out 130KHZ switching noise.	Across R329 (22k) piggyback a 4700pf capacitor of the same size directly solder	Add this capacitor in parallel with short traces. No re-spin yet.	C.1	C.0

Table 1. MPC8572DS (Whitefin) Corrected Errata/Enhancement Requests

#	Error/ Type	Problem/Request	Errata Correction		Assy Rev	Schem Rev
			Work-around	Re-spin Resolution		
9	CE9	Fix an IR drop problem for a thermal diode measuring circuit.	1. Remove C850 (Leave Do not Populate) capacitor. 2. Add two 30 A.W.G. wires running from R567/R568 pads to the depopulated C850 pads. a. One wire runs from {depopulated C850 pin 1 pad on the "TEMP_CATHODE" Net} to {R568 pin 2 pad on the "TEMP_CATHODE" Net}. Short as possible, but can accommodate ICT. Glue to board. Runs parallel to the "TEMP_CATHODE" Net, thus adds additional copper to that net. b. One wire runs from {depopulated C850 pin 2 pad on the "TEMP_ANODE" Net} to {R567 pin 2 pad on the "TEMP_ANODE" Net}. Short as possible, but can accommodate ICT. Glue to board. Runs parallel to the "TEMP_ANODE" Net, thus adds additional copper to that net.	Keep C850 as a "do not populate". Widen traces for nets TEMP CATHODE and TEMP_ANODE to 15 to 20 mils. No re-spin yet.	C.1	C.0
10	UE1	ATX mounting holes did not include copper ring on top AND bottom layer for screws.	None	Corrected	X5	NA

Table 1. MPC8572DS (Whitefin) Corrected Errata/Enhancement Requests

#	Error/ Type	Problem/Request	Errata Correction		Assy Rev	Schem Rev
			Work-around	Re-spin Resolution		
11	UE2	3.3V LED is incorrectly connected to HOT3.3V	Document that this LED is really indicating Hot 3.3V	Routed R505 to 3.3V instead of Hot 3.3V	X5	C.0
12	UE3	Local Bus Extensive voltage ringing due to too fast of edge rate of the TI LATCH U27 and U28 on bus LB_A_FS<0..31>	None	Added series resistors 1230-1231 to reduce ultra-fast edge rate.	X5	C.0
13	ER2	When in endpoint mode, cannot get into AC97 mode for ULI M1575.	None	Added a resistor R1232 option to pin C29 of the ULI audio section to pull to ground to select AC97.	X5	C.0
14	ER3	For ASM bring up, it is preferred to have two serial ports.	None	Added J100 header. Needs a simple custom cable. Workbook and Schematics have details.	X5	C.0
15	ER4	Need mounting holes within PCB boarder so that board can be retested by ICT as a field return.	None	Added to rails per product engineering.	X5	NA
16	ER5	Add additional fraducials top and bottom for assembly.	None	Added	X5	NA
17	ER6	U31 and U26 geometry too narrow.	None	Library and PCB corrected	X5	NA
18	ER7	FPGA. Add another Aux register to allow tracking of DDR input clock	Added Aux2 register at map offset 0x08 created version 0.2 for rev X4 or earlier (rev A or B PCB) and version 1.0 for rev X5 or later (rev C or D PCB).	Same	X5 Earlier ver if flashed.	NA

3 UNCORRECTED ERRATA or ENHANCEMENT REQUESTS

The changes listed below are either errata which cannot be implemented on the current version of the board, or are requests for enhancements to the board that have not been implemented. These changes *may* be addressed in a revised version of the board, if any more should occur. These track issues and desires for future designs to address. Freescale Semiconductor does not warrant that these issues/requests will ever be addressed.

.

Table 2. MPC8572DS (Whitefin) Uncorrectable Errata or Enhancement Requests

#	Eng. Errata #	Problem or Enhancement	Respin Solution
1	ER1	Reference Clock to SGMII add-in card.	Hook up at least one REFCLK to SGMII connector. Future use.
2	UE4	Nets LDTRST* and PWROK* (reserved pins AL20 and AL21 should have been pulled up to VDD_ENET_IO (2.5V) instead of 3.3V. Does not cause improper operation but maybe best for long term reliability	route both pullups to VDD_ENET_IO (2.5V) instead of 3.3V. No respin yet.
3	UE5	LB_GPL<4> should not be connected to U42 or U47 flash devices. It was an incorrect assumption that the timing could work for the RDY/BSY pins for these flashes.Does not cause improper operation. But functionality is not benefitial and is incorrect usage.	Remove connection and routing of LB_GPL<4> to U42 and U47. No respin yet.

4 Revision History

Rev	Date	Changes
1	2007 Nov. 1	Initial Errata
2	2008 APR 24	Added CE8- CE9
2.1	2008 APR 24	Added UE4-UE5

THIS PAGE INTENTIONALLY LEFT BLANK

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 010 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
+1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Document Number: MPC8572DS
Rev. 2.1
4/2008