Flip Chip Plastic Ball Grid Array (FC-PBGA)

Application Note

Q2 2012

FC-PBGA Application Note

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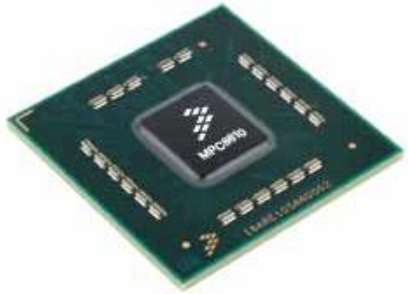
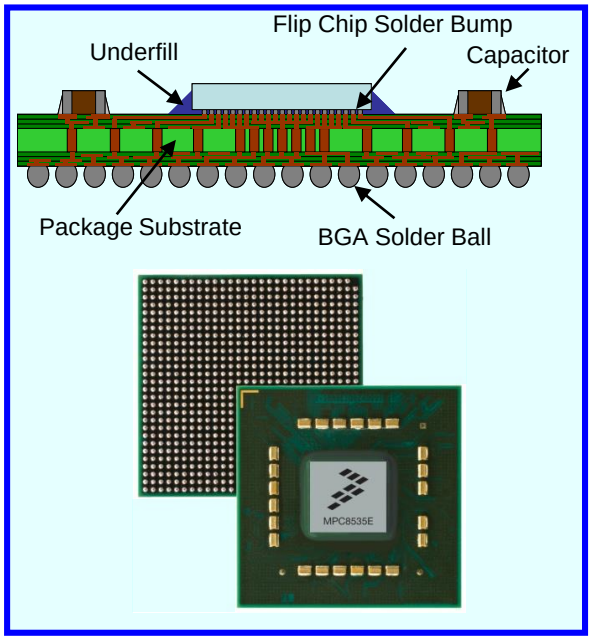


FC-PBGA Package Configurations

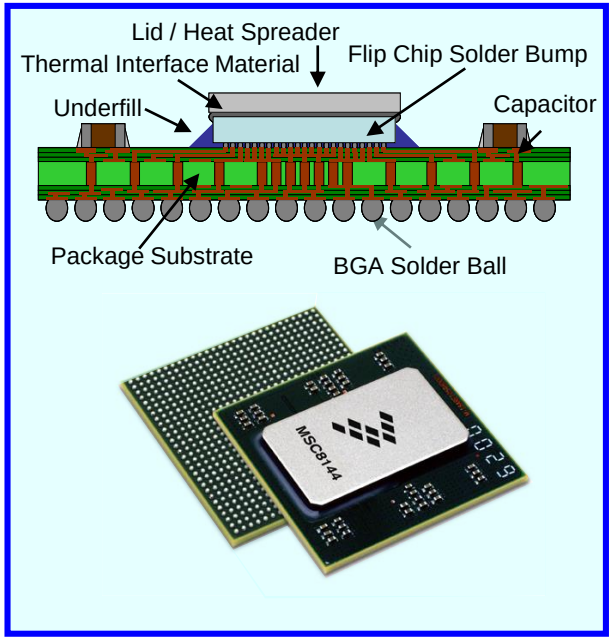
Freescale Flip Chip Package Configurations

Many Freescale high performance products require the performance advantages of a flip chip Ball Grid Array (BGA) package. Flip chip packages are offered in bare die, flat lid and full lid configurations.

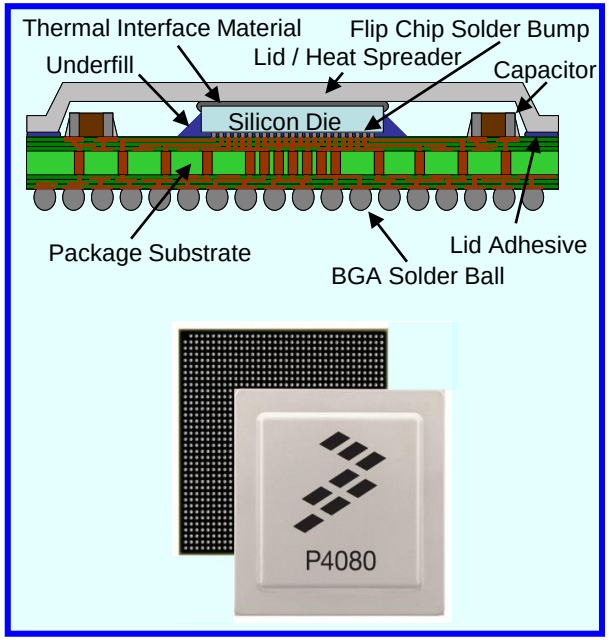
Bare Die Configuration



Flat Lid Configuration



Full Lid Configuration

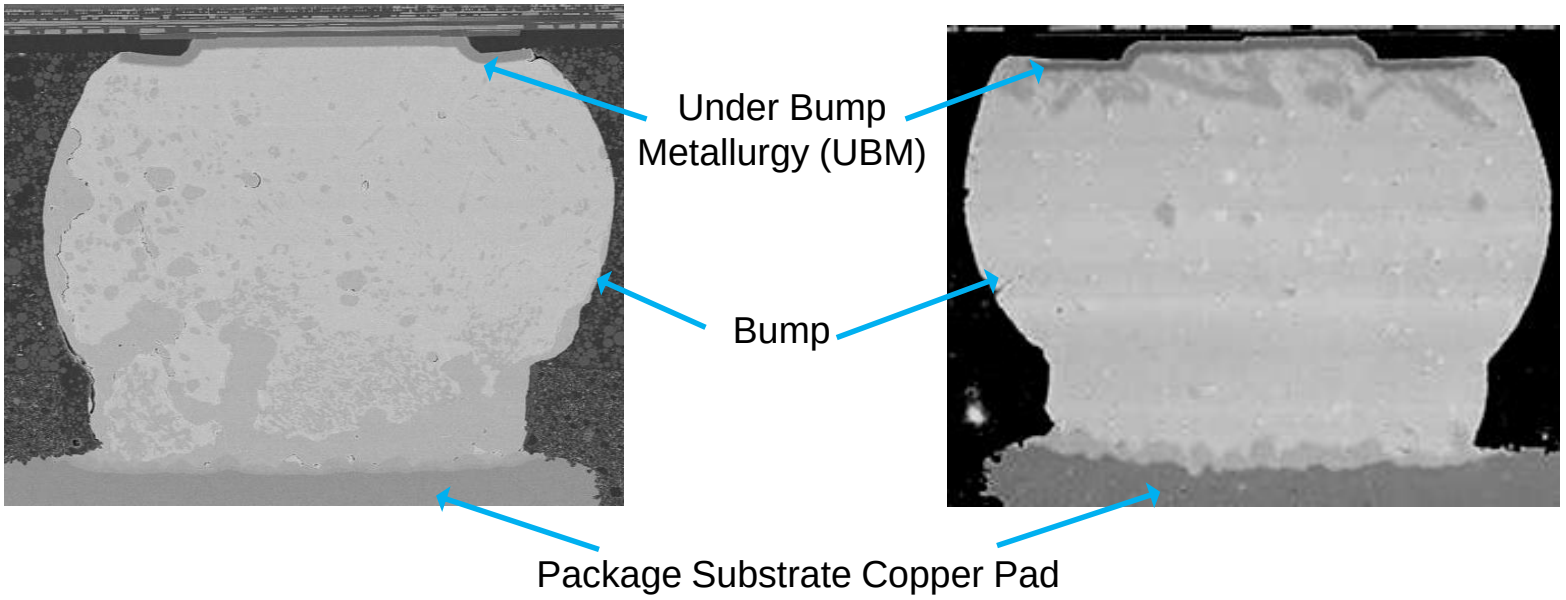


Freescale FC-PBGA Solder Bump Construction

Freescale FC-PBGA packages feature either a high-lead solder bump soldered to the package substrate with a eutectic tin-lead solder or a lead-free bump

Typical High-Lead Solder Bump Interconnect

Typical Pb-Free Solder Bump Interconnect



Freescale FC-PBGA Body Sizes

- Freescale Flip-Chip PBGA body sizes range from 17x17mm to 45x45mm
- BGA sphere pitch currently ranges from 0.8 to 1.27 mm

Freescale Flip-Chip PBGA Package Attributes

Body Size (mm)	Package I/O Count	Sphere Pitch (mm)	Sphere Array	Pkg SM Diam* (mm)
17x17	332	0.8	19x19	0.4
20x20	431	0.8	23x23	0.4
21x21	520	0.8	25x25	0.5
21x21	624	0.8	25x25	0.525
23x23	780	0.8	28x28	0.5
21x21	255	1.27	16x16	0.635
25x25	360	1.27	19x19	0.635
25x25	575	1.0	24x24	0.55
29x29	783	1.0	28x28	0.55
33x33	1023	1.0	32x32	0.55
37.5x37.5	1295	1.0	36x36	0.55
45x45	1935	1.0	44x44	0.55

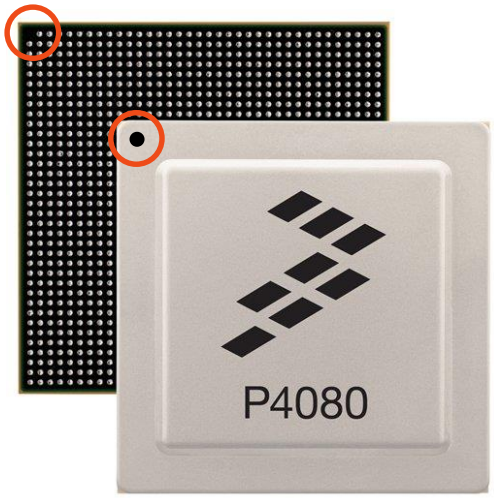
* Package BGA pads are soldermask defined. "Pkg SM Diam" is the BGA pad soldermask opening

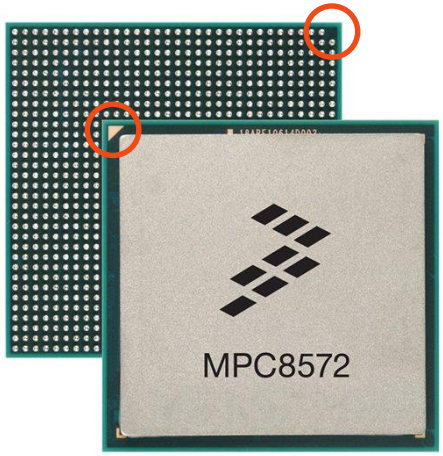
- *Information is based on products currently in production and is subject to change.*
- *Contact Freescale or visit www.Freescale.com for details on specific products.*

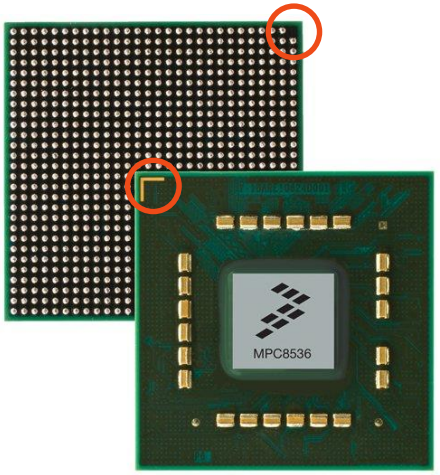
FC-PBGA Pin A1 Location

Pin A1 location on Freescale devices may be indicated by a topside marker and/or depopulated corner sphere on the bottom-side

Examples of Pin A1 Markers



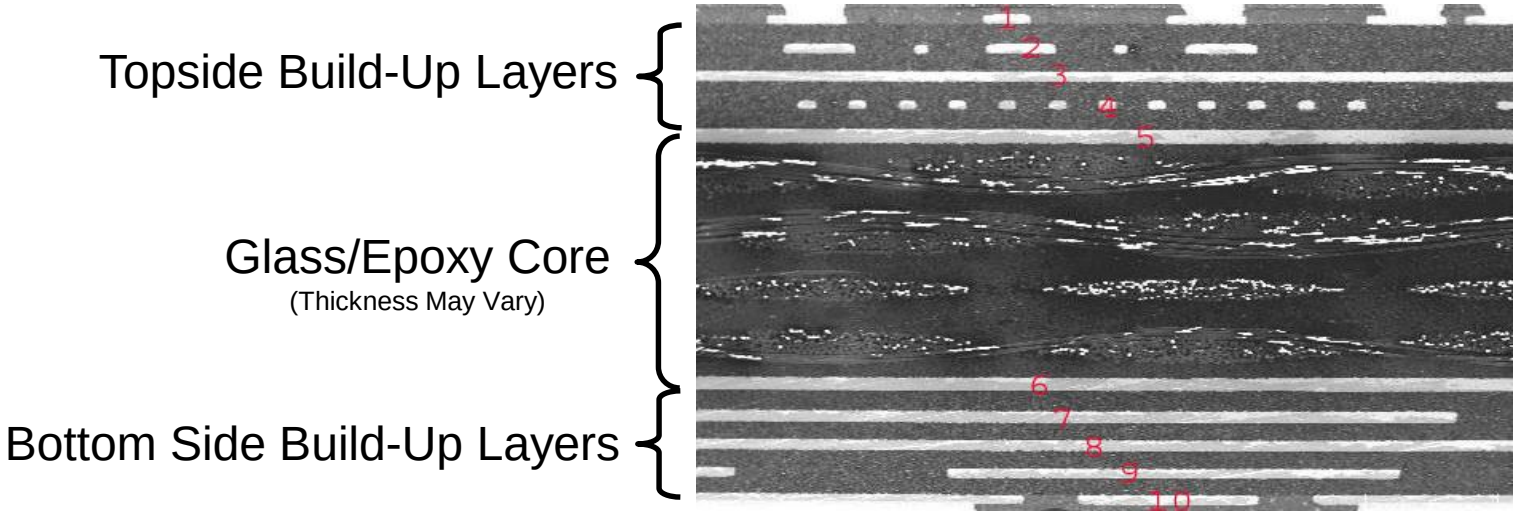




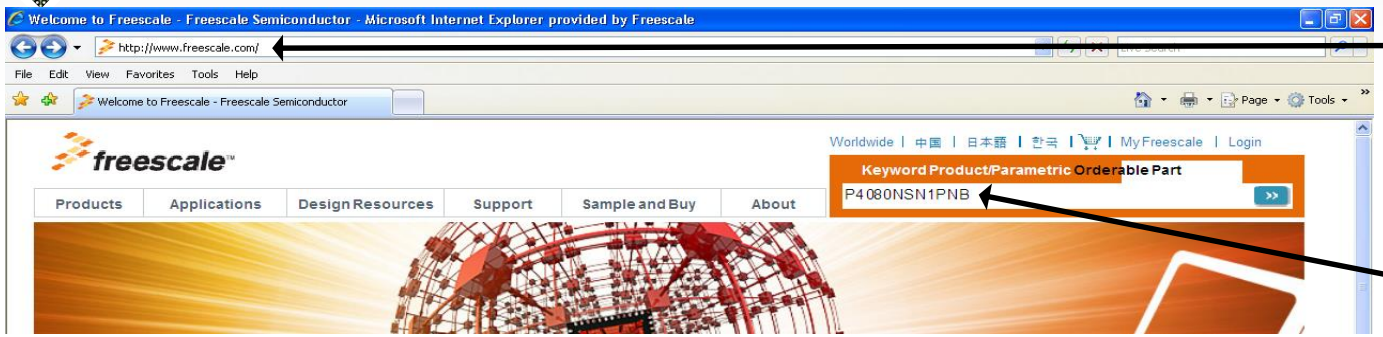
FC-PBGA Substrate Construction

- Most FC-PBGA substrates feature High Density Interconnect (HDI) construction with Build-Up (BU) layers on both sides of glass/epoxy core.
- Construction is typically designated by the number of build-up and core copper layers (BU-C-BU)
  - Example: (3-2-3) construction is 3 build-up layers on both sides of a two layer glass/epoxy core
- See Freescale package drawings for substrate thickness specifications

10-Layer (4-2-4) Construction Cross-Section

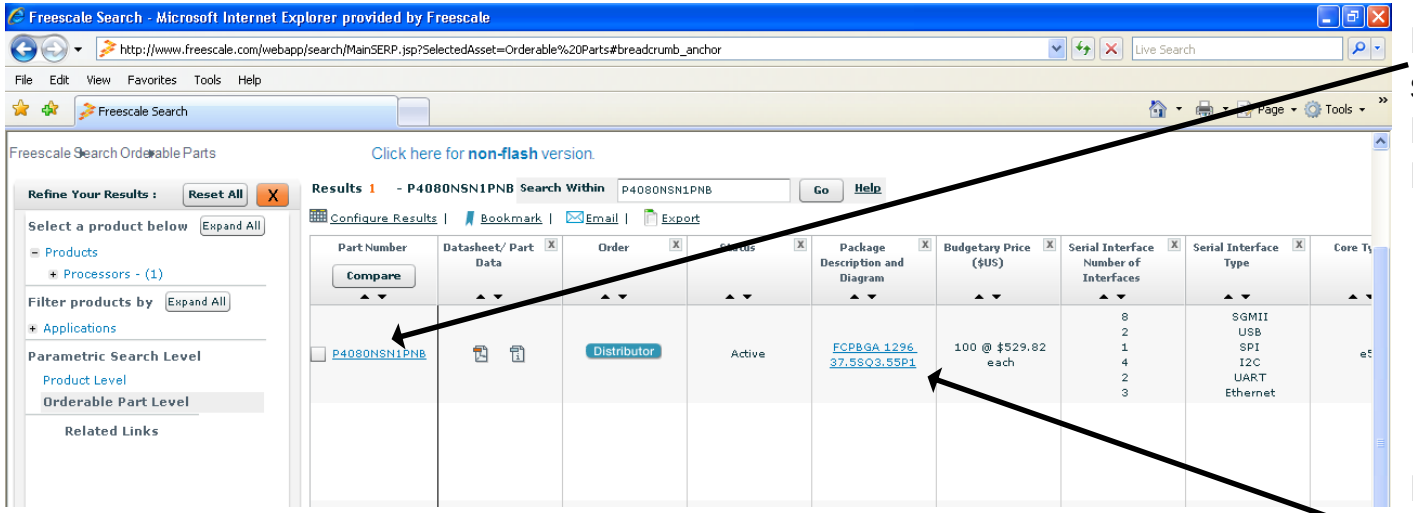


Freescale Package Drawing Location



Go to : http://www.freescale.com/

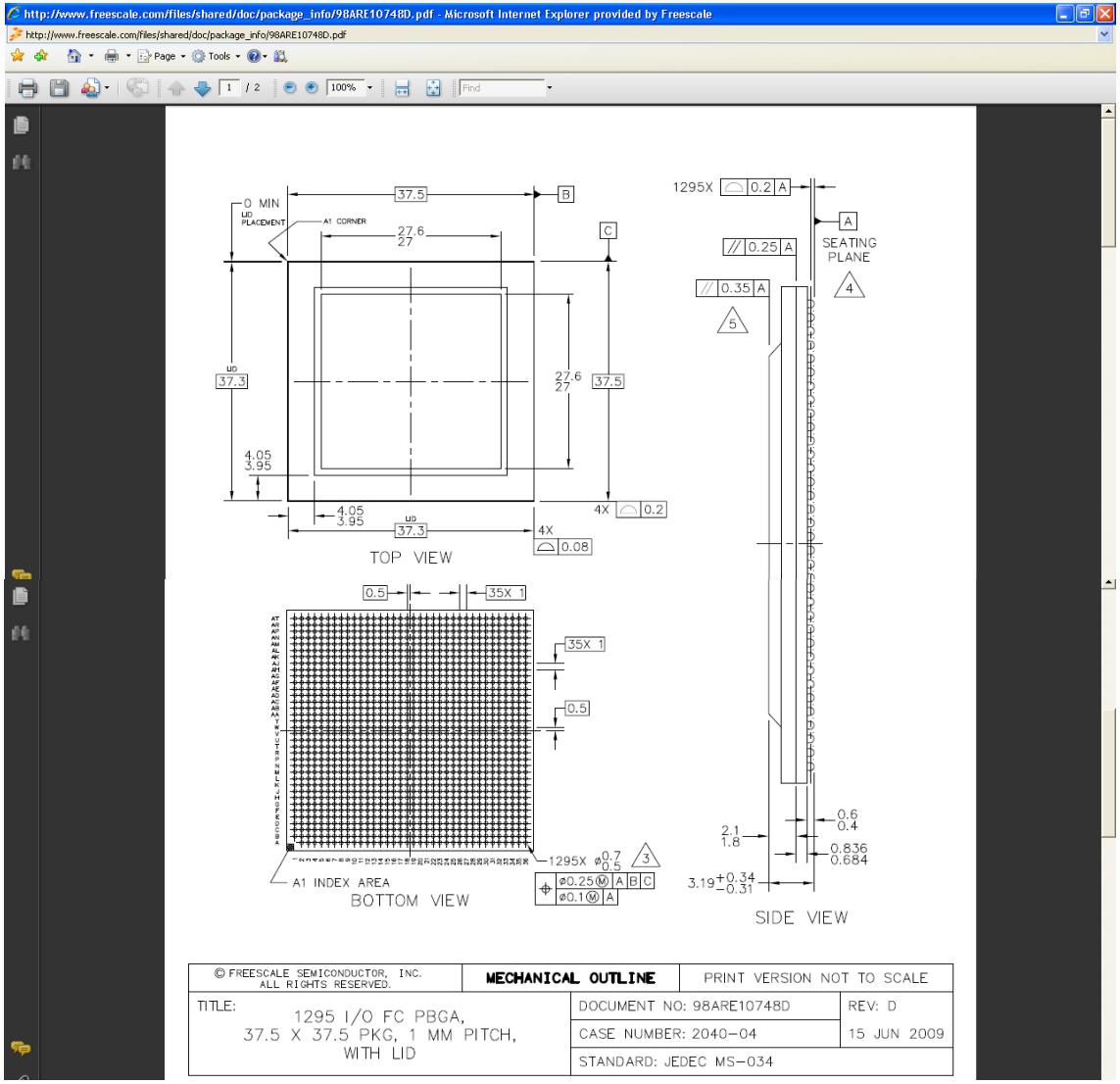
Enter Part Number. P4080NSN1PNB is used for this example



Next screen shows search results for Part Number P4080NSN1PNB

Package drawing can at found at this link (see next slide)

Example 1296 Lidded FC–PBGA Package Drawing

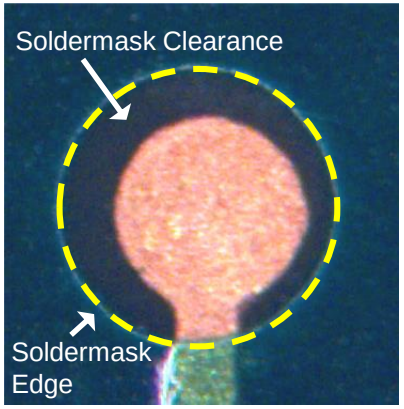


Printed Circuit Board Design for FC-PBGA

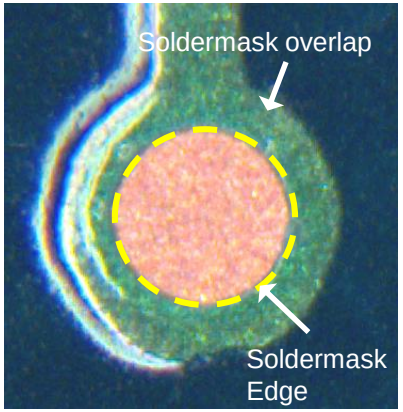
Printed Circuit Board Pad Design for FC-PBGA

- **Solder pad diameter:**
  - In general, printed circuit board (PCB) pad solderable diameter should match the package pad diameter
    - See table on slide 6 for common package pad diameters
  - When required for routing, motherboard pad diameter may be decreased by up to 10% versus the package pad
- **Solder pad configurations:**
  - Non-Soldermask Defined (NSMD) pads:
    - Most common type of motherboard pad in the industry
    - Typically results in the most consistent solderability, especially with hot air solder leveled (HASL) surface finish
  - Soldermask Defined (SMD) pads:
    - Added strength provided by the soldermask overlap
  - NSMD motherboard pads recommended for most applications

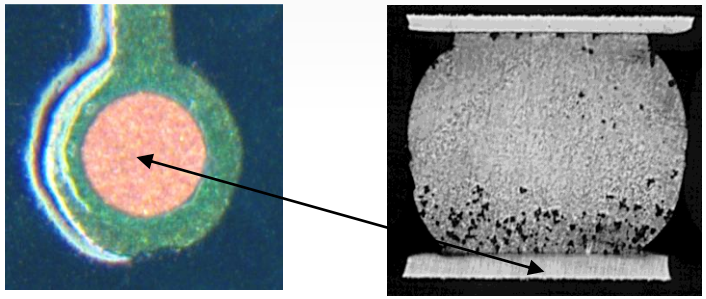
NSMD Pad



SMD Pad



Trade-Offs Between SMD and NSMD PCB Pads



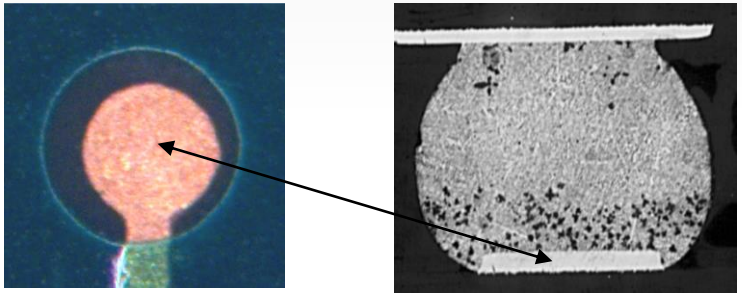
SMD = SolderMask Defined

Advantages

1. Strongest mechanical strength
2. More copper, better heat spreading to board
3. More heat resistant - multiple reworks

Disadvantages

1. Potential stress point
2. Foreign matter entrapment on pad
3. Possible worse dimensional tolerance on solderable diameter versus NSMD



NSMD = Non-SolderMask Defined

Advantages

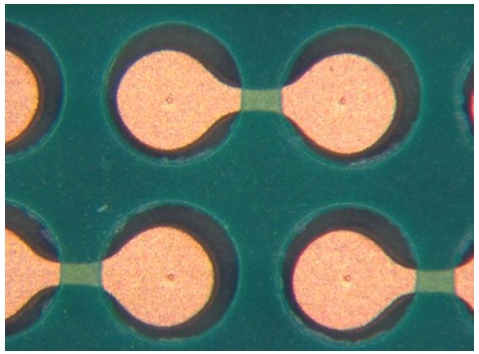
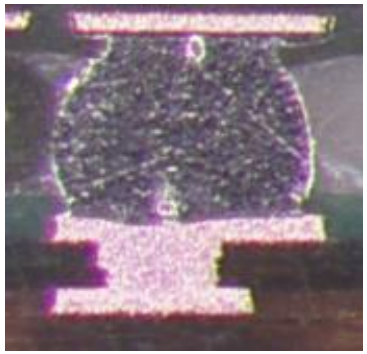
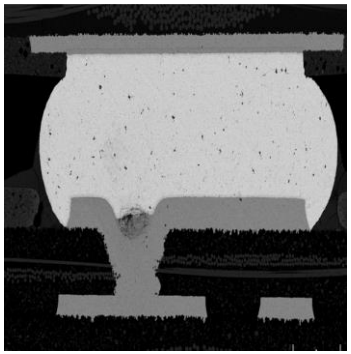
1. Most common pad configuration
2. Potentially the most solderable pad since no soldermask encroachment
3. No point of stress concentration at PC board
4. More copper to copper space to route traces between pads

Disadvantages

1. Reduced pad to PCB adhesion strength
2. May be weak link in other mechanical testing, i.e. board bending, mechanical shock and vibration
3. Non-symmetrical joint fails at the package interface first in thermal cycling

PCB Pad Design Guidelines

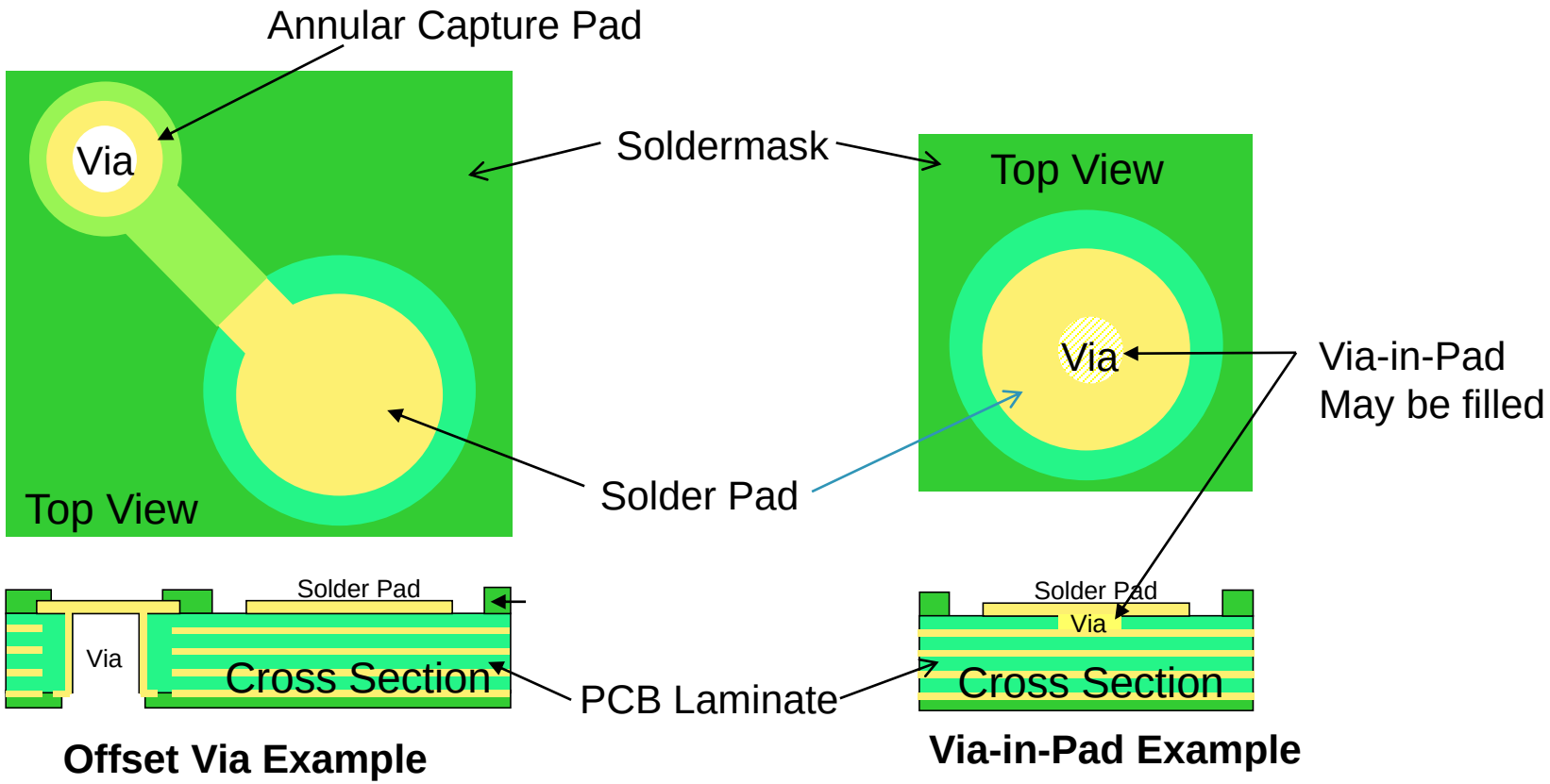
- **PCB Surface Finish for FC-PBGA**
  - Surface finishes compatible with FC-PBGA include: organic solderability protectant (OSP), Hot Air Solder Leveled (HASL), electroless or electrolytic nickel/gold (NiAu) and immersion silver (Ag)
- **PCB Routing Vias for FC-PBGA**
  - For coarser BGA pitches, use thru-hole vias that are offset from the BGA PCB pad and placed interstitially between BGA pads
    - Via preferably tented with soldermask on both sides of PCB or soldermask covering the trace connecting the via and BGA pad
  - Finer pitches may require the use of via-in-pad structures:

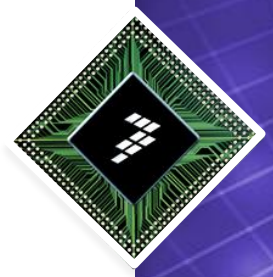
PCB Pads for PBGA Employing MicroVia-in-Pad
(Use of plated or otherwise filled microvias recommended)

PCB Pad Design for FC-PBGA

- Diameter of Copper Solder Pad shown below should be equal to or as much as 10% smaller than FC-PBGA package pad diameter (see Slide 6 for package diameters)



Surface Mount Assembly



Surface Mount Assembly

Avoiding FC-PBGA Package Delamination

- Always follow instructions on shipping container
- Do not exceed the package peak temperature (PPT) rating shown on the shipping container label
  - Example: An MSL3 245ºC device can only be out of the original vacuum sealed dry bag one week (i.e., 168 hours) maximum prior to soldering, and the peak package temperature should not exceed 245C during reflow.
- Establish strict process control and procedures to ensure safe operation conditions
- Use dry nitrogen cabinets to store devices after opening packages
- Rework boards within time allowed in room environment
  - Example: An MSL3 device must be soldered and reworked within one week of opening the vacuum sealed dry bag
- FC-PBGAs that have been out of the dry bag longer than their specified MSL rating can be baked dry at 125ºC for 24 hrs. This is highly recommended prior to any rework or removal of the FC-PBGA from the PCB

Surface Mount Assembly

FC-PBGA Pre-Assembly Handling

- FC-PBGAs are typically moisture sensitive and rated at MSL3 following JEDEC moisture sensitivity specifications in J-STD-020, similar to other plastic packages.
  - Follow Moisture Sensitivity guidelines printed on the package labels.

JEDEC Moisture Level Table		
Level	**Condition**	**Allowable Time Out of Dry Pack***
1	30°C / 85% RH	Unlimited
2	30°C / 60% RH	1 year
2a	30°C / 60% RH	4 weeks
3	30°C / 60% RH	168 hours
4	30°C / 60% RH	72 hours
5	30°C / 60% RH	48 hours
5a	30°C / 60% RH	24 hours
6	30°C / 60% RH	Time on Label

***Re-Bake required if time our of Dry-Pack exceeds allowable limits**

Surface Mount Assembly

Solder Stencils:

- For BGA the typical stencil aperture diameter should be the same size as the PCB solder pad
- Slight reductions (0.02 - 0.05 mm) of the stencil diameter to the PCB pad diameter may improve gasketing between the stencil and the PCB and help with solder paste release
- 125 to 150 μm thick stencils have been found to give good results
- Follow the IPC-7525 *Stencil Design Guidelines*

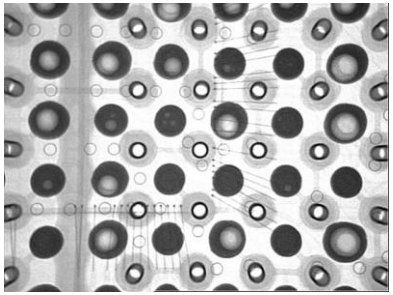
Solder Paste:

- Use of no clean rosin based solder paste is recommended
- For 0.65 mm BGA solder ball pitch and higher use a paste formulated with type 3 powder
- For BGA pitches below 0.65 mm type 4 powder is recommended

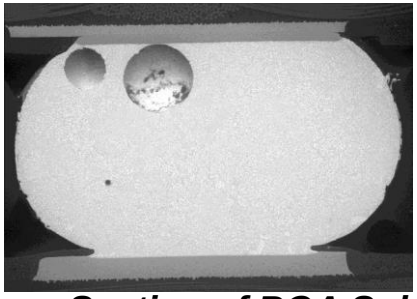
Surface Mount Assembly

FC-PBGA Solder Joint Voids

- BGA solder joint voids commonly known as “Macro” or “Process” voids are the result of solder paste flux volatiles trapped during the solidification of the molten solder during the PCB reflow assembly process
- PCB assembly process parameters as well as the type of solder paste used can have a significant impact on the quantity and size of the voids.
- Water washable solder paste typically produces larger voids than rosin based paste
- IPC-610 calls out a void criteria of 25% of joint area
  - Studies* have shown no quality or reliability issues with voids ≥25%



X-Ray Showing Voids in BGA Solder Joints



Cross-Section of BGA Solder Joint Showing Macro Voids

Reference: "The Effects of Solder Joint Voiding on Plastic Ball Grid Array Reliability,“ Donald R. Banks, et al., 1996 SMI Proceedings, pages 121-126.

Surface Mount Assembly

FC-PBGA Placement

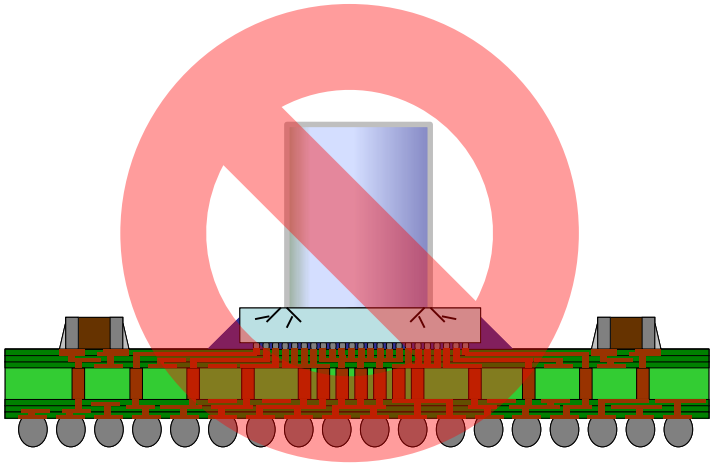
- FC-PBGAs have excellent self-centering properties which are attributed to surface tension between the applied solder on the PCB solder pad and the FC-PBGA solder sphere
- FC-PBGA solder spheres can be placed up to 50% off the PCB pad
  - Surface tension during solder reflow will center the BGA spheres to the PCB pads.
- Placement machine vision systems can be used to place the FC-PBGA by either sphere alignment or component package body alignment
- When placing by component body alignment the solder sphere location variability is typically +/- 0.075 mm, worst case
- The solder spheres of the FC-PBGA should be pushed into the printed solder paste until contacting the PCB solder pad to reduce the risk of HIP (Head in Pillow) open solder joints

Surface Mount Assembly

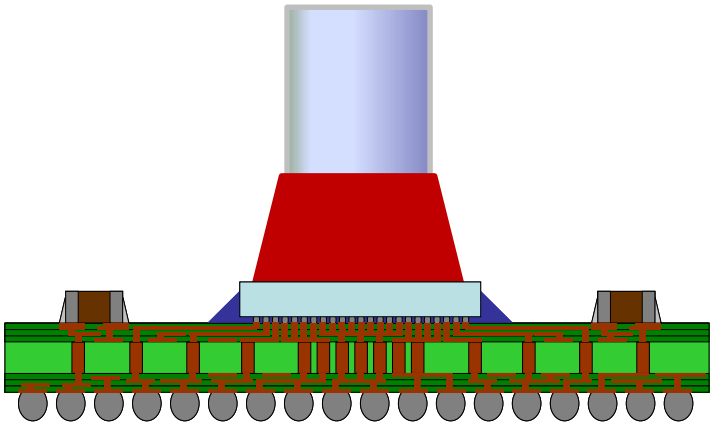
FC-PBGA Placement – Bare Die Packages

- Care should be taken to avoid damaging the exposed silicon die backside or edges when handling and placing bare die devices. A compliant tip nozzle (such as rubber), preferably with closed loop head force control should be used to pick and place exposed silicon devices
- Consult your pick and place equipment provider for pick-up tip size and material recommendations.

Metal Pick-Up Tip May Cause Damage to Exposed Die



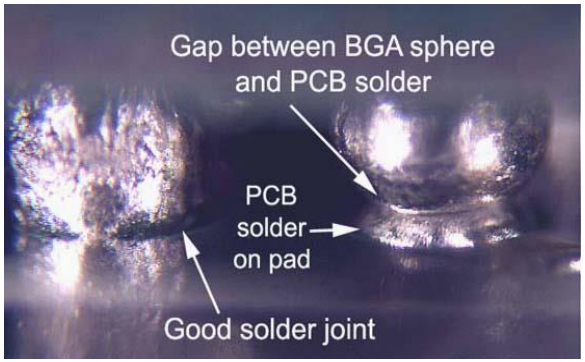
Compliant Tip Nozzle is Preferred



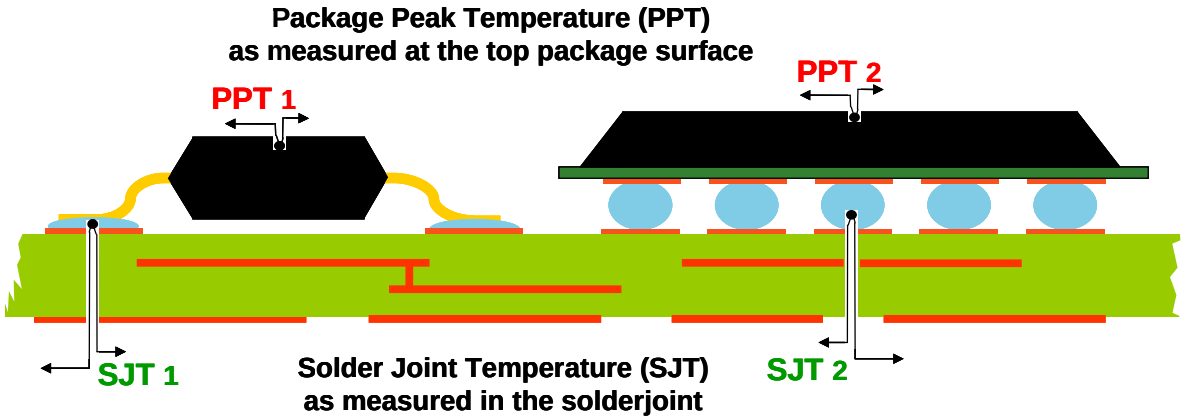
Surface Mount Assembly

Soldering Pb-Free BGA with Pb-Free Solder Paste - Reflow Recommendations

- Reflow preheat - Use the solder paste suppliers minimum reflow preheat recommendations to avoid over drying of the paste flux which can contribute to “Head in Pillow” (HIP) open solder joints
- Achieve a minimum solder joint temperature (SJT) of 235ºC
  - Ideal peak temperature is typically 240 – 245C
- Dwell time above 217ºC should be 50 – 80 seconds



Head In Pillow (HiP) Open Joint

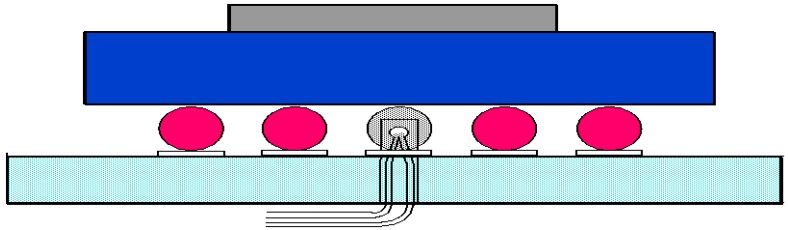


Package Peak Temperature vs Solder Joint Temperature

Surface Mount Assembly

Thermal Profiling Recommendations

- Use new, fine gauge, calibrated, welded thermocouple beads
  - 36 gage wire preferable
- Hand twisted thermocouple wires can cause inaccurate readings
  - Temperature will be taken at first good contact twist or shared with several contact points
- For FC-PBGA, embed the thermocouple which will measure the SJT (solder joint temperature) in the solder sphere using high temperature, thermally conductive, electrically insulative epoxy
- Larger FC-PBGAs can have a high thermal mass relative to other components and should be carefully profiled with one thermocouple in a corner sphere and a second thermocouple in a inner sphere on a fully populated profile PCB



Surface Mount Assembly

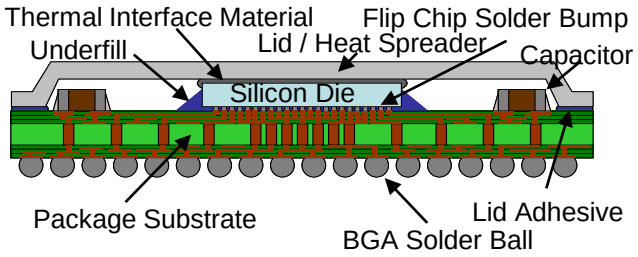
Soldering Pb-free BGA with SnPb Solder Paste

- In some applications, it may be required that BGA with Pb-free spheres may need to be soldered using traditional SnPb soldering processes
- Such mixed alloy BGA soldering processes are not typically recommended
- A minimum solder joint temperature (SJT) of 225ºC may be used to provide for complete melting of the BGA solder sphere and mixing with the SnPb solder paste
- Dwell time above the solder paste melting temperature of 183ºC should still be 50 – 80 seconds
- Use the solder paste supplier's minimum reflow preheat recommendations to avoid over drying of the paste flux which can contribute to "Head in Pillow" (HIP) open solder joints
- Before board assembly verify all components on the PCB can withstand package peak temperatures (PPT) >225ºC

Surface Mount Assembly

Post Reflow Washing

- Post reflow washing with water or solvents is typically discouraged as moisture or chemicals could corrode or attack package materials
- If a water or solvent wash process is used, care must be taken to completely dry the water from the PCB and components following the wash process
  - Component should be cooler than wash fluid when entering wash process
- This is especially true with the full lid FC-PBGA configuration shown below
  - This configuration typically features venting that allows pressure equalization between the inside and outside surfaces of the lid
- During the water or solvent wash process, moisture or chemicals may seep under the lid through the vents
  - To remove this moisture a post-wash bake is strongly recommended.



Typical Full Lid FC-PBGA

Surface Mount Assembly

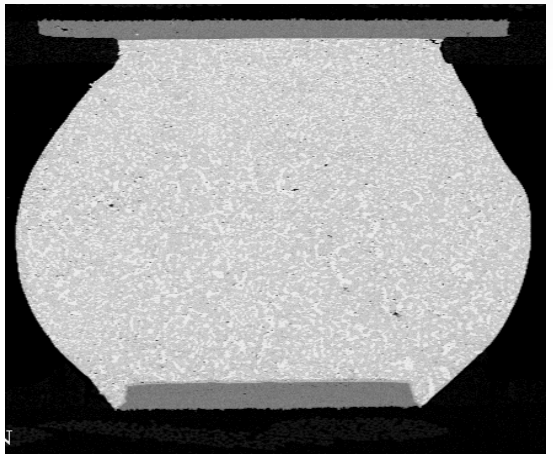
FC-PBGA Sphere Alloys

- FC-PBGA solder spheres may be Pb-bearing or Pb-free
  - All BGA spheres should collapse to the PCB solder pad during assembly soldering
  - The amount of collapse is controlled by solder pad geometries and surface tension of the solder

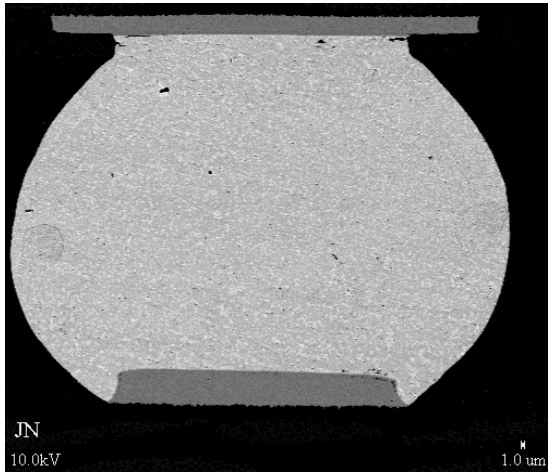
- Pb-bearing sphere compositions may include:
  - The most common is 62Sn36Pb2Ag
  - Some may contain 63Sn37Pb

- Lead-free sphere compositions may include:
  - SAC387 - 95.5Sn3.8Ag0.7Cu
  - SAC405 - 95.5Sn4.0Ag0.5Cu
  - SAC305 - 96.5Sn3.0Ag0.5Cu
  - SnAg - 96.5Sn3.5Ag

Note:
1) Pb = lead, Sn = tin, Ag = silver, Cu = copper
2) All compositions listed are weight percent



SnPbAg PBGA Sphere



SAC405 PBGA Sphere

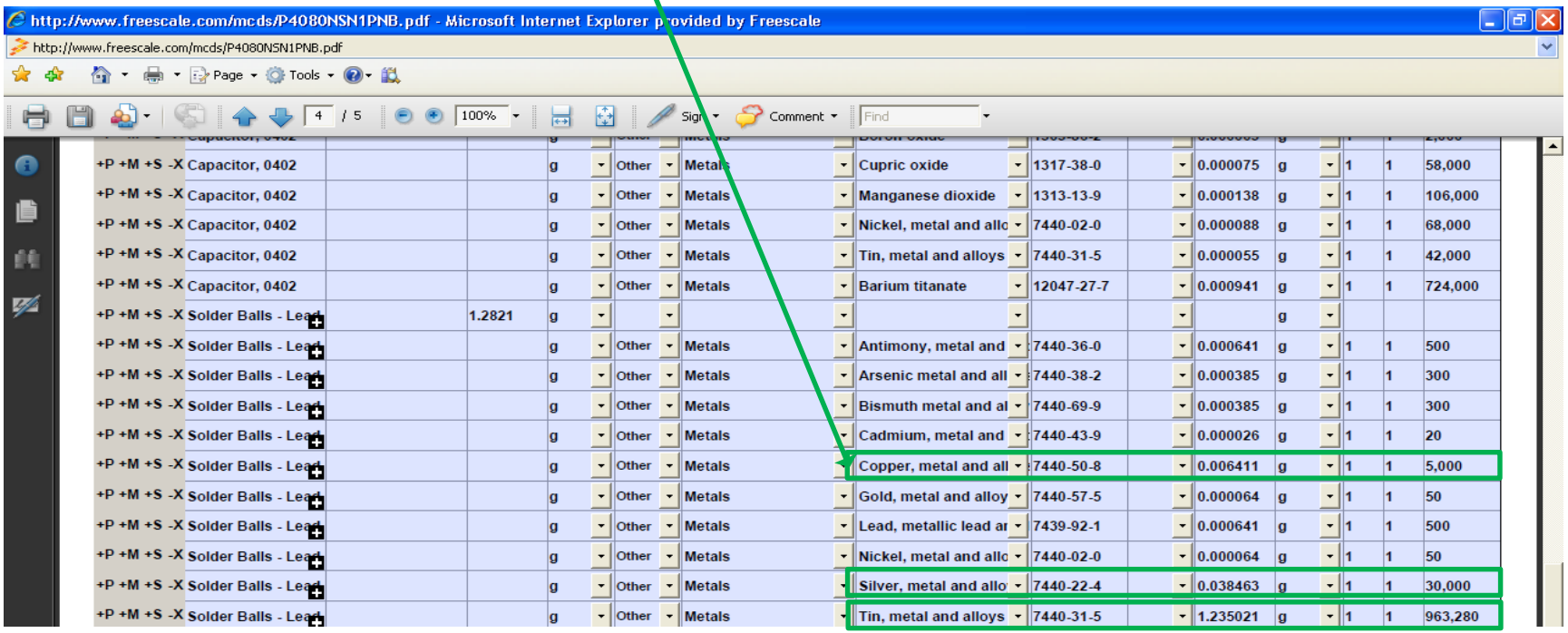
Surface Mount Assembly

FC-PBGA Rework

- Entire board to be reworked should be baked for at least 12 hours at 125° C or the highest temp the assembly can withstand to remove moisture which can result in FC-PBGA package delamination
- FCPBGA spheres completely melt and will solder without additional solder if flux only is applied. Solder paste is not required for FC-PBGA replacement
- The same careful temperature profiling procedures should be used for rework as is used during the original reflow process
- Preheat the entire board in an offline bake oven to minimize “oil canning” type PCB warpage under the FC-PBGA. Preheat SnPb soldered boards to a minimum of 125ºC and Pb-free boards to a minimum of 150ºC
- After desoldering the FC-PBGA remove residual solder from the PCB solder pads while the PCB is still hot using solder wick and a soldering iron
- Apply a small volume of no clean flux to the cleaned PCB solder pads
- Place the new BGA using a microscope or rework station that incorporates a vision system capable of viewing the BGA spheres as well as the PCB solder pads
- It is not recommended to use reballed BGAs on products due to long-term solder joint reliability concerns

Determining FC-PBGA Solder Sphere Alloy

- Following the instructions on slide 9, go to http://www.freescale.com/
- Enter the Freescale Part Number (make sure “Orderable Part” is selected)
- On the next screen, click on the link for package drawing which will open a table
- Click on “Download IPC-1752 Report” which opens the Matl Composition Report
- The solder sphere alloy including maximum allowable trace elements will be listed
- In this example the alloy is SAC305 or 96.5%Sn3.0%Ag0.5%Cu by weight



Component Level Qualification

FC-PBGA Component Level Qualification

- Flip-Chip PBGA packages are typically qualified to industrial tier levels based on JEDEC specifications
- Most Flip-Chip PBGA packages are qualified to MSL3 at peak reflow of either 245ºC or 260ºC
  - Products qualified to MSL3 must be soldered within 168 hours after opening dry-pack

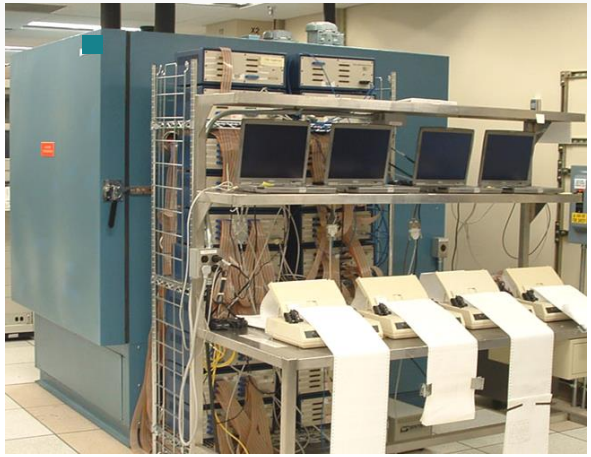
Typical Flip-Chip PBGA Industrial Qualification Levels

Environmental Stress	Condition	With Precondition?	Qualification Readpoint	JEDEC Reference
Moisture Preconditioning - Level 3	30 C, 60% RH, 196hrs + 3x Reflow			J-STD-020C
Air to Air Temperature Cycle (AATC)	-40 to 125 C	Yes	850 Cycles	JESD22-A104
	OR			
	-55 to 125 C	Yes	700 Cycles	
High Temperature Storage (HTS)	150 C	No	1008 Hours	JESD22-A103
Perform Either ONE of the Following:				
Temperature-Humidity Bias (THB)	85 C, 85% RH	Yes	1008 Hours	JESD22-A108
Biased Highly Accelerated Stress Test (Biased HAST)	130 C, 85% RH	Yes	96 Hours	JESD22-A110

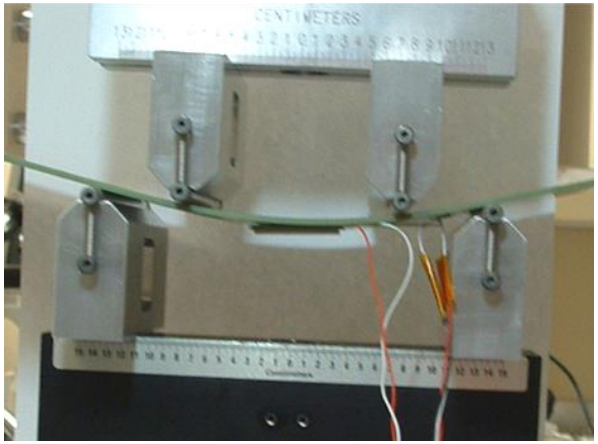
FC-PBGA Board Level Reliability

FC-PBGA Board Level Reliability

- Board mounted thermal cycling solder-joint reliability performed per IPC-9701A
  - Printed Circuit Board
    - 0.093” thick, 8 Cu layers
    - NSMD pads, OSP finish
  - Air Temperature Cycling
    - 0/100ºC, 10 minute ramps, 10 minute dwells
    - In-situ daisy chain resistance monitoring
      - 300 Ohms or greater is considered a failure
- Board mounted monotonic bend to failure performed per IPC-9702
  - Printed Circuit Board
    - 0.093” thick, 8 Cu layers
    - NSMD pads, OSP finish
  - Bend Test
    - Bend at strain rate of 5000 microstrain/second
    - Failure is break in strain/continuity



Single Chamber Thermal Cycling

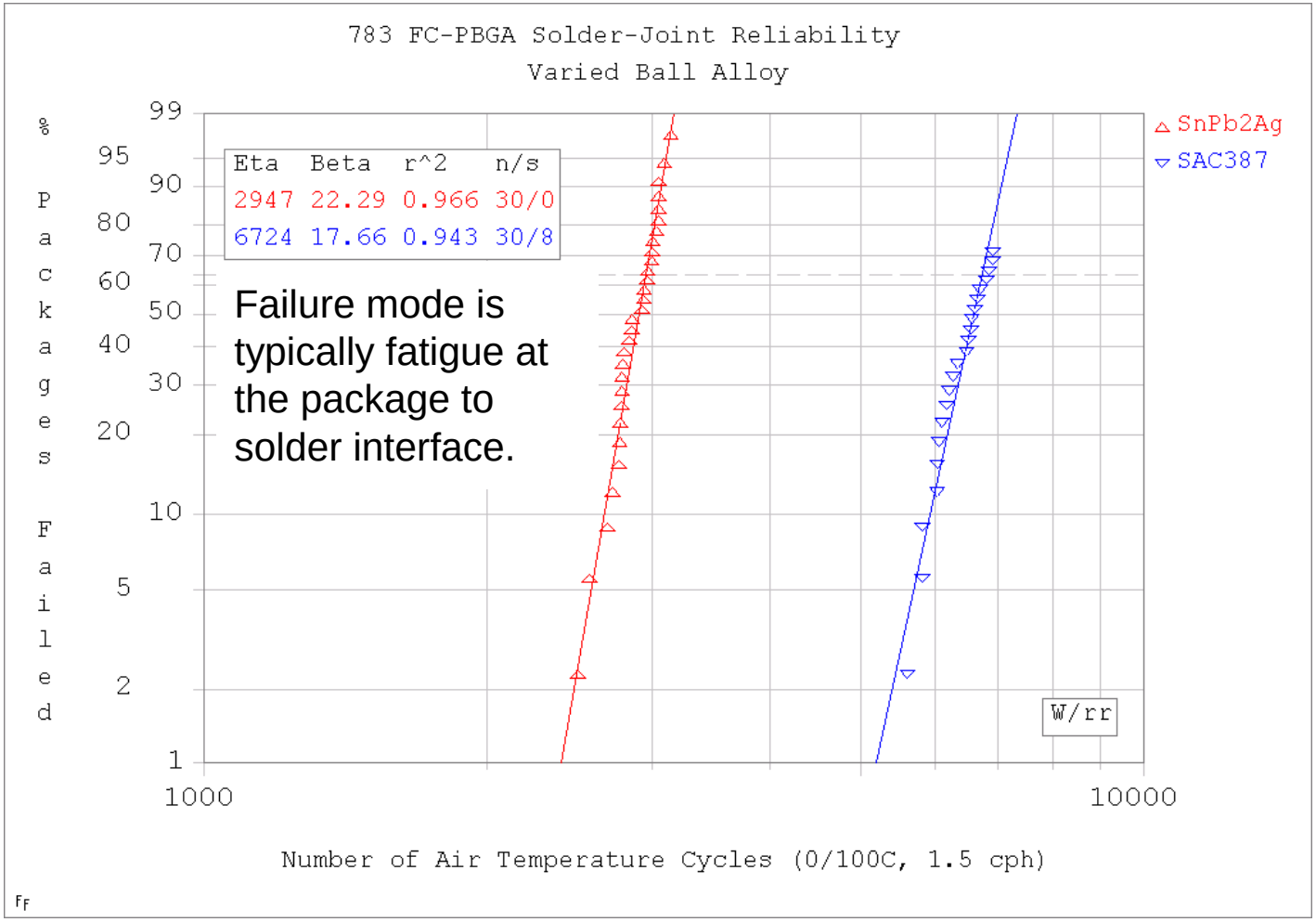


Monotonic Bend to Failure Testing

FC-PBGA Board Level Reliability

Example: FC-PBGA Board-Level Thermal Cycling Reliability

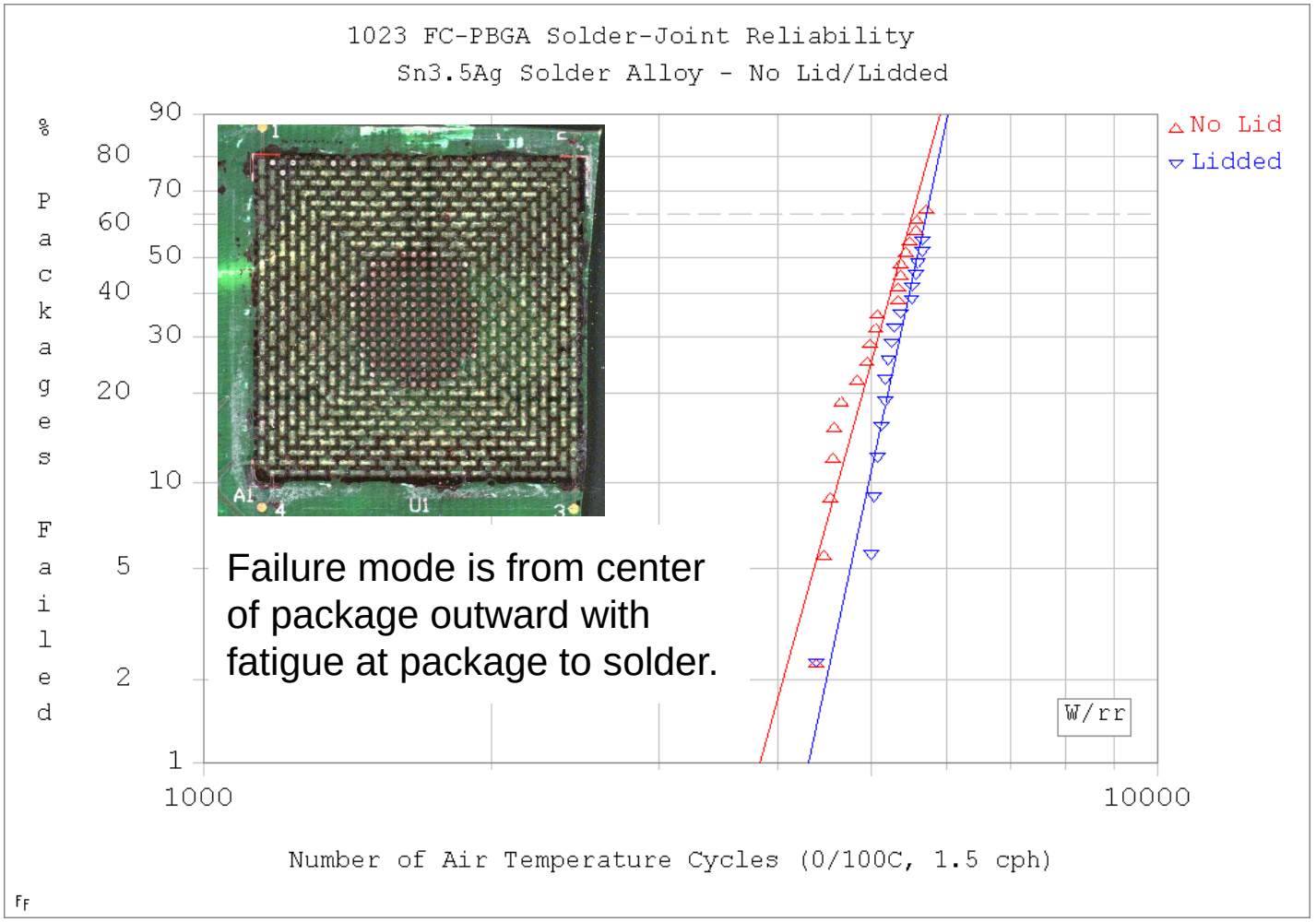
Sphere Alloy Comparison



FC-PBGA Board Level Reliability

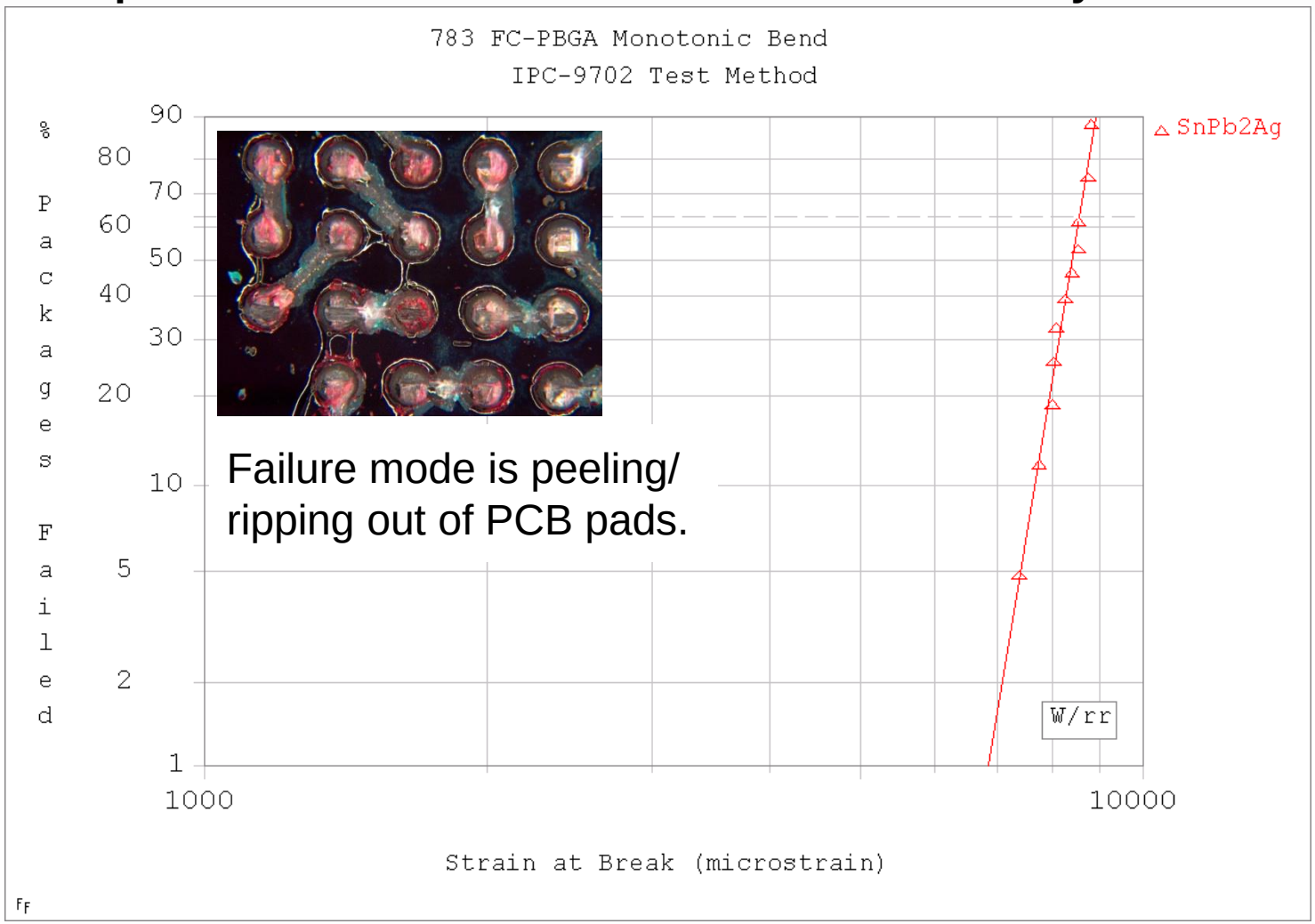
Example: FC-PBGA Board-Level Thermal Cycling Reliability

Lid Configuration Comparison



FC-PBGA Board Level Reliability

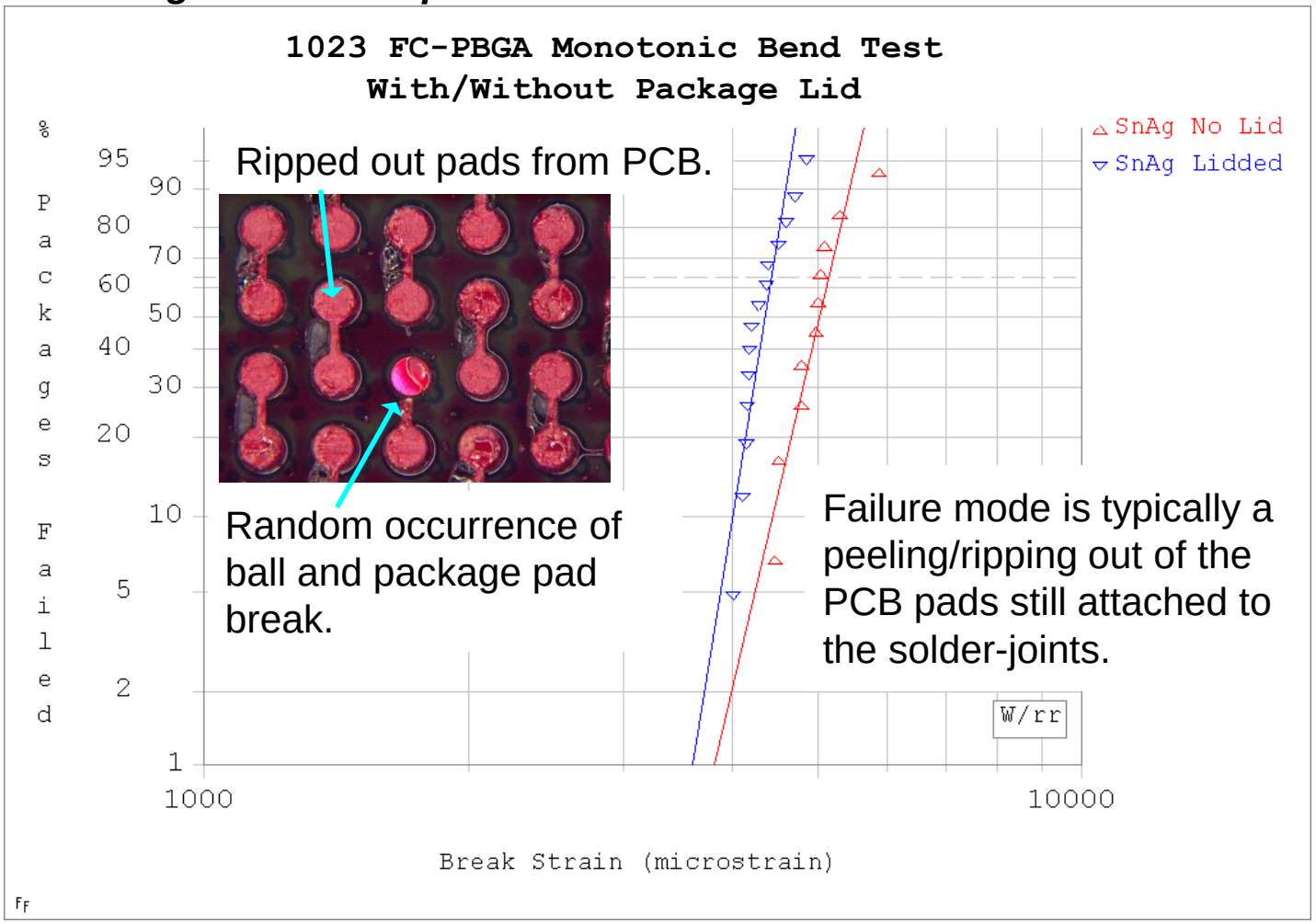
Example: FC-PBGA Board-Level Bend Test Reliability



FC-PBGA Board Level Reliability

Example: FC-PBGA Board-Level Bend Test Reliability

Lid Configuration Comparison



FC-PBGA Board Level Reliability

- Freescale routinely gathers solder-joint reliability data for FC-PBGA packages
  - Data taken using IPC-9701A and IPC-9702 test methods
- Testing is by package configuration
  - For example, many Freescale products use the 783 FC-PBGA package
- Data availability
  - For packages not shown, customers may request reports from the appropriate Freescale Sales office or Freescale Applications group

FC-PBGA Thermal Performance

FC-PBGA Thermal Performance

Typical FC-PBGA Thermal Resistances in Standard JEDEC Environment:

- **Example Case for 783 FC-PBGA 29x29 mm Body with Lid**

Table of Thermal Resistance Data

Thermal Metric	JEDEC Test Board		Value	Unit
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	18	°C/W
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	13	°C/W
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	12	°C/W
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	9	°C/W
Junction to Board		$R_{\theta JB}$	5	°C/W
Junction to Case (Top)		$R_{\theta JCtop}$	0.6	°C/W

Notes:

1. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
2. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

FC-PBGA Thermal Performance

Typical FC-PBGA Thermal Resistances in Standard JEDEC Environment:

- **Example Case for 624 FC-PBGA 21x21 mm Body with No-Lid**

Table of Thermal Resistance Data

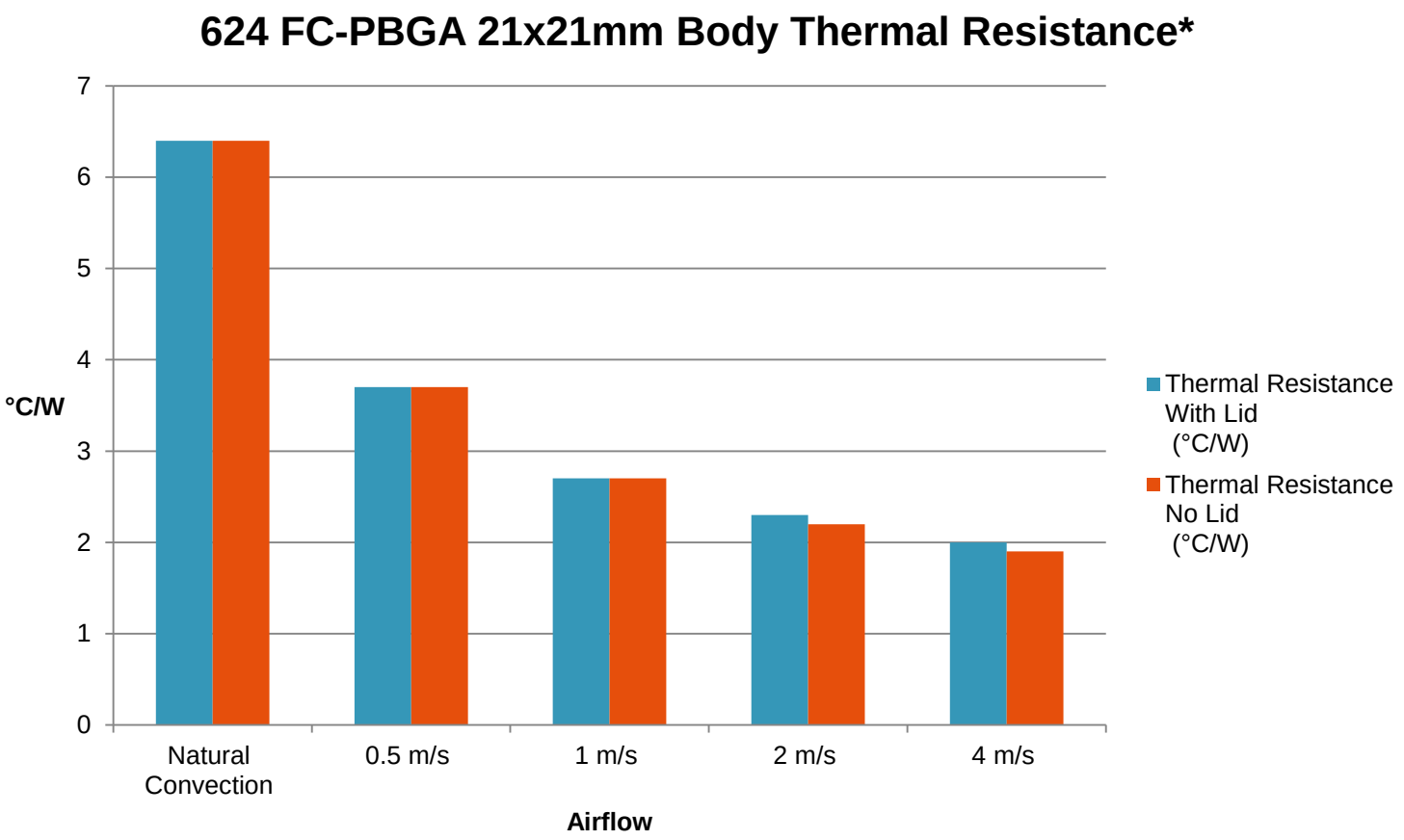
Rating			No Lid	Unit
Junction to Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	31	°C/W
Junction to Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	22	°C/W
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	24	°C/W
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	18	°C/W
Junction to Board		$R_{\theta JB}$	12	°C/W
Junction to Case (Top)		$R_{\theta JCtop}$	< 0.1	°C/W

Notes:

1. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
2. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

FC-PBGA Thermal Performance

Comparison of Lid vs. No-Lid FC-PBGA Thermal Resistances:



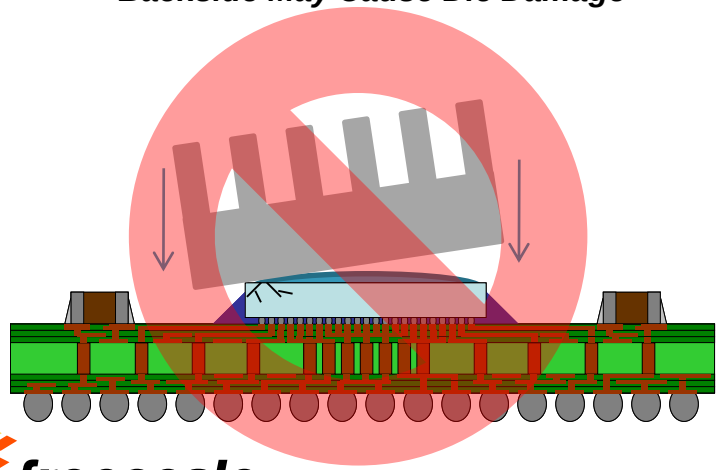
*53 x 53 x 25 mm Pin Fin HeatSink

FC-PBGA Thermal Performance

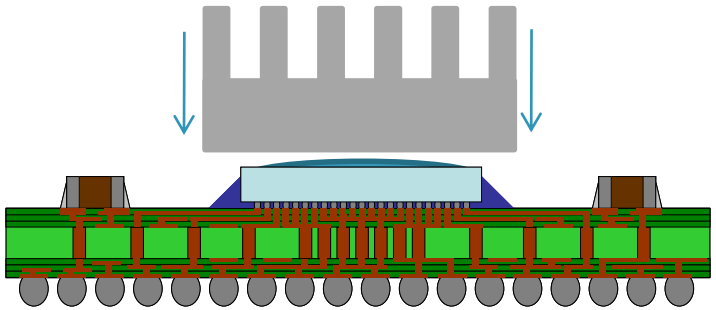
Thermally Sinking Lid-Less Flip Chip Devices

- A uniform layer of thermal interface material must be present between the heat sink and the exposed die. Heat sink must not directly contact exposed die surface.
- Heat sink must be brought in contact with die backside thermal interface material with surface parallel to exposed die. Direct contact with die edges and corners may result in die damage
- Thermal Interface Material is not a glue and should not be relied upon exclusively for adhesion

Application of Heatsink Non-Parallel to Die Backside May Cause Die Damage



Heatsink Surface Should be Parallel to Die BackSide Surface



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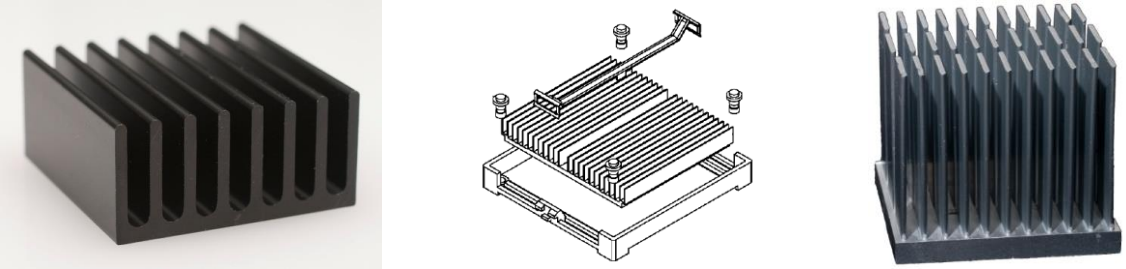
FC-PBGA Thermal Performance

Heat Sink Attachment

- The maximum allowable junction temperature for each product can be typically found in the hardware specification
- Depending on the application and the Freescale product involved, most applications may require a heat sink
  - The heat sink is selected by the customer
- It is recommended that heat sinks be attached to the Printed Circuit Board (PCB)
  - Clipping or attaching to the FC-PBGA substrate can result in solder ball failure
  - Backing plate may be necessary to prevent board warpage
- Maximum allowable heat sink attachment force varies by product and is typically as high as 45 Newtons (10 lb force)



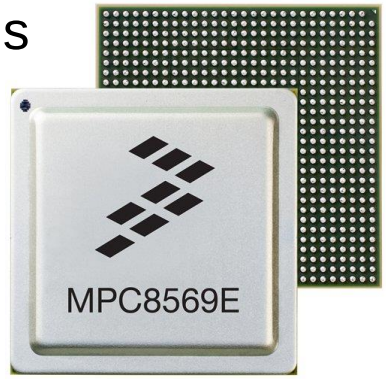
Examples of Package Heat Sinks Available in the Industry

FC-PBGA Thermal Performance

System-Level Thermal Modeling

Example Case for 783 FC-PBGA with Full-Footed Lid in Network Server Application

- Package: 783 29x29 mm FC-PBGA with fully footed lid
- Typical configuration considered: Four 783 FC-PBGA parts each on 3 AMC* cards, 27 mm gap between cards
- Air speed 2 m/s
- Inlet air temperature: 55ºC
- Each board uses an extruded plate fin heat sink (70×118×19 mm) to cool all FC-PBGA parts
- FC-PBGA device power is temperature dependent, power increases with temperature
  - Careful design of cooling system critical to prevent thermal runaway

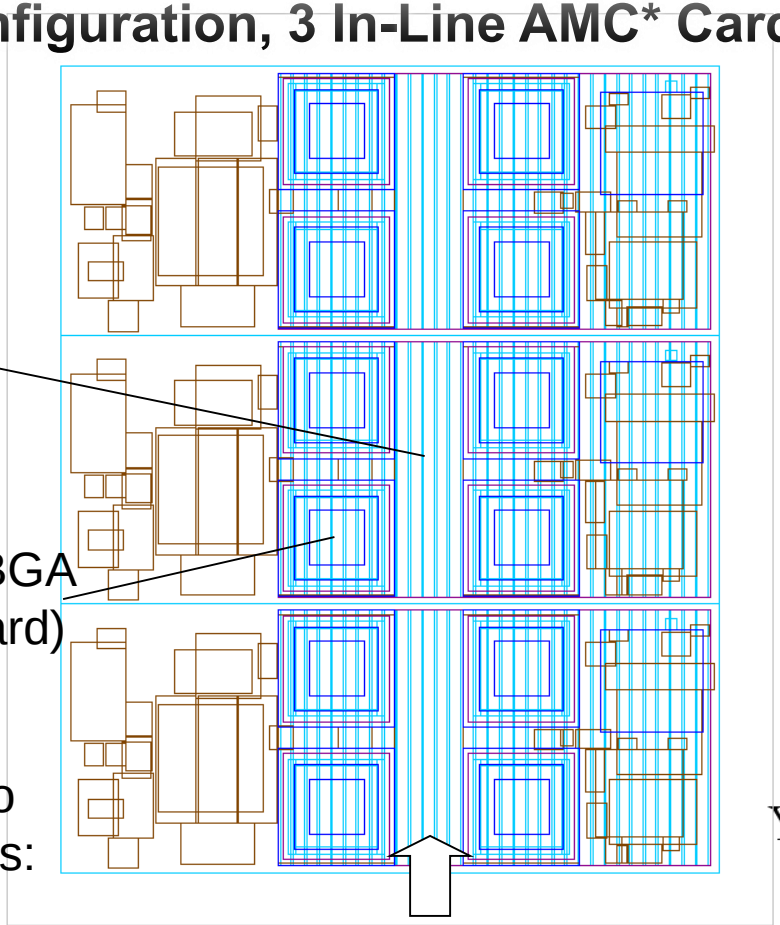


783 FC-PBGA

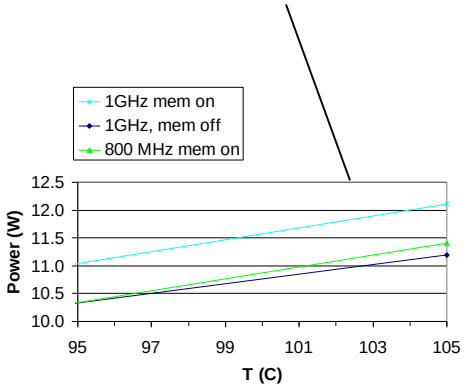
Note: AMC = Advanced Mezzanine Card

FC-PBGA Thermal Performance

Front View of System Thermal Model
In-line Configuration, 3 In-Line AMC* Cards



Device Power is Temperature Dependent

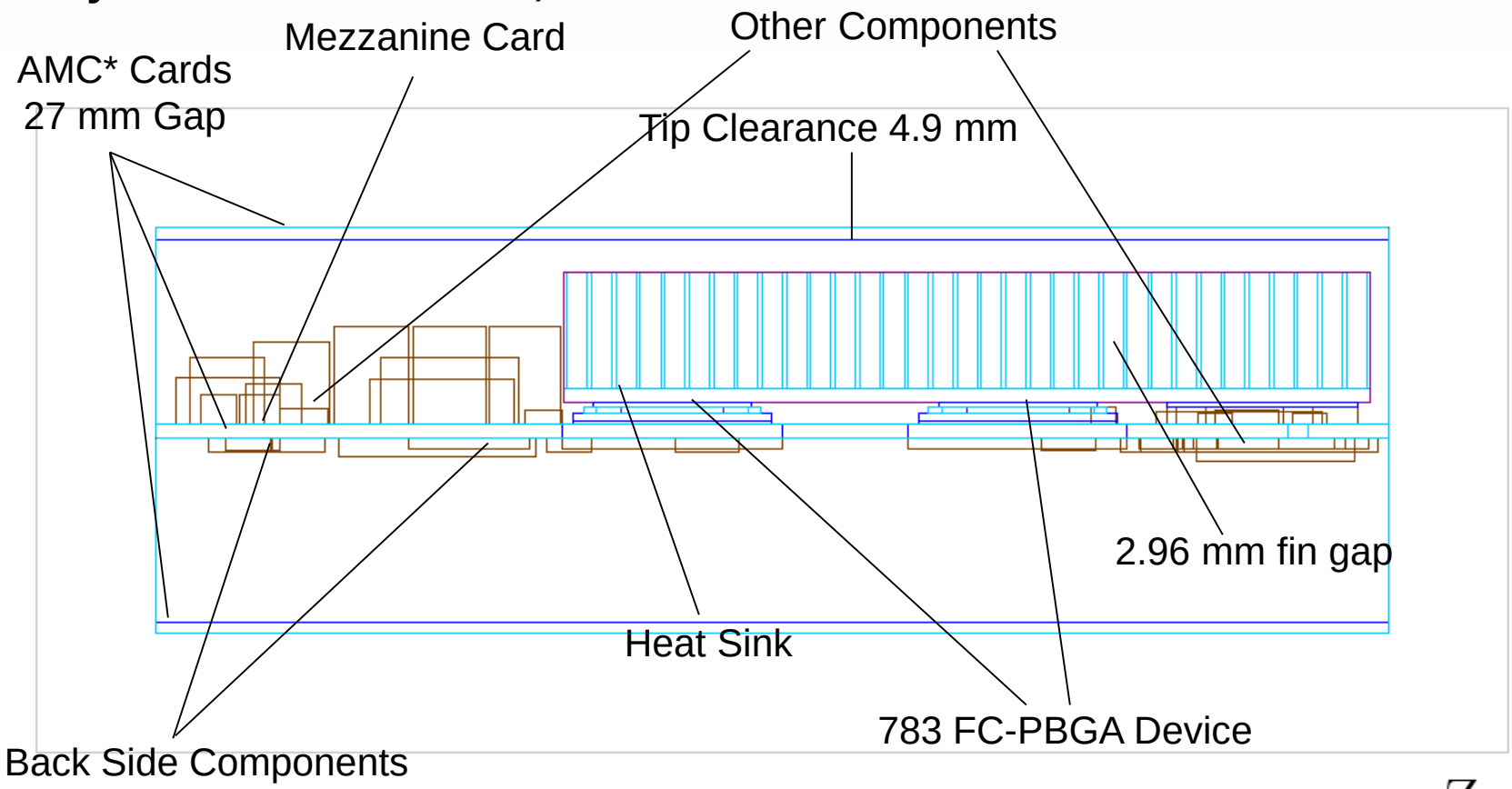


2 m/s Air Flow, T inlet = 55ºC

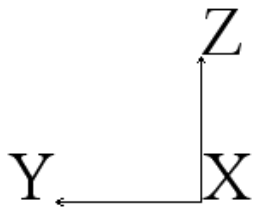
Note: AMC = Advanced Mezzanine Card

FC-PBGA Thermal Performance

System Thermal Model, End View



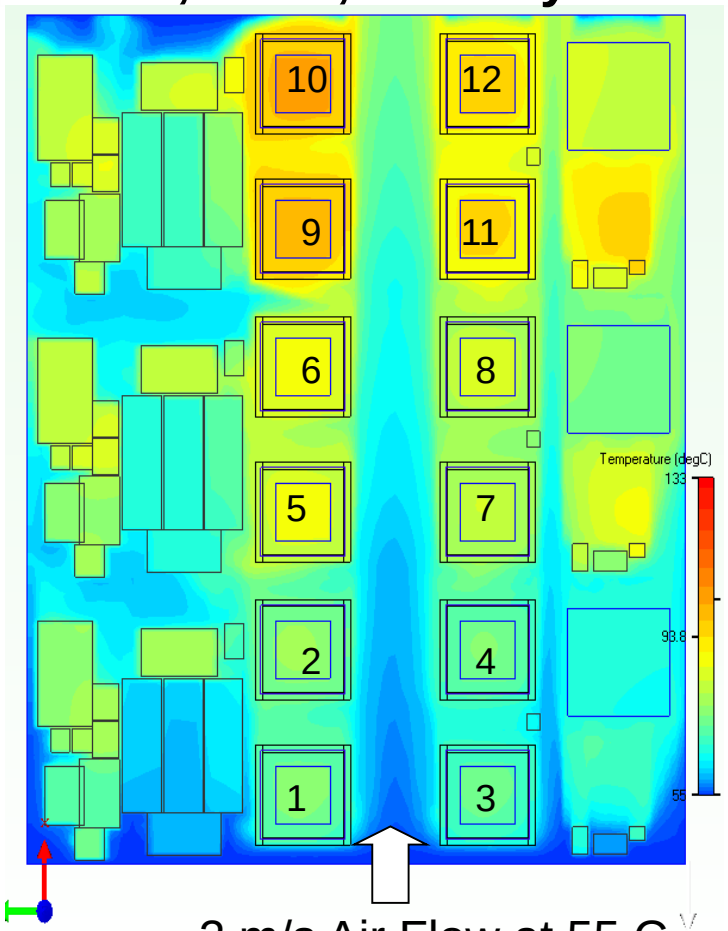
Note: AMC = Advanced Mezzanine Card



FC-PBGA Thermal Performance

Die Temperature Plot, In-Line Configuration 3 Cards, 4 Parts per Card, 1Ghz, Memory On

g



All parts work within 105ºC junction temperature

FC-PBGA power range: 9.1-12W

Device power is temperature dependent

Total Power due to other Components: 15.1 W per Card

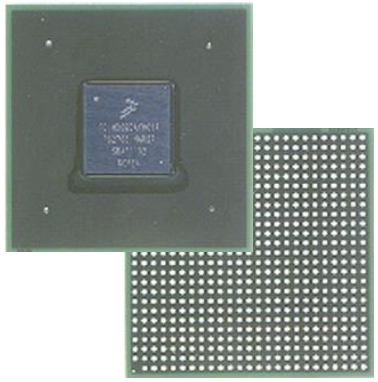
Position	T junction (C)	Power (W)
1	74.7	9.1
2	77.2	9.2
3	72.2	8.8
4	74.4	8.9
5	87.7	10.5
6	89.6	10.5
7	83.1	10.0
8	84.9	10.0
9	100.7	12.0
10	102.9	12.0
11	94.5	11.3
12	96.3	11.3

FC-PBGA Thermal Performance

System-Level Thermal Modeling

Example Case for 624 FC-PBGA Non-Lidded in Netbook Application

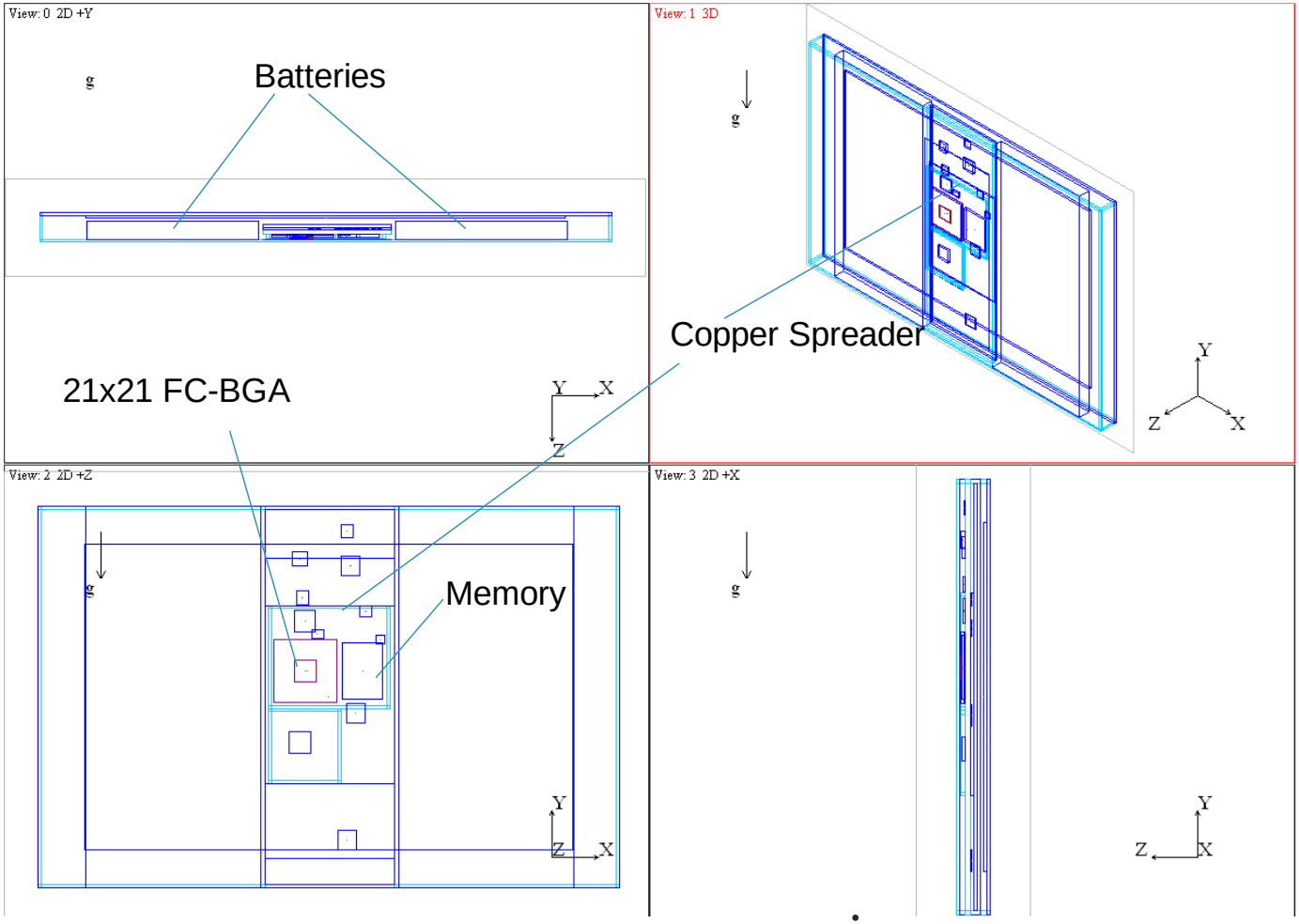
- Package: 624 21x21mm FC-BGA (no lid)
- Typical netbook design, including board, components, thermal management solution
- Box size: 200x130x10 mm (Approximate)
- Board size: 40x125x1.6 mm (Approximate)
- No airflow



624 FC-PBGA

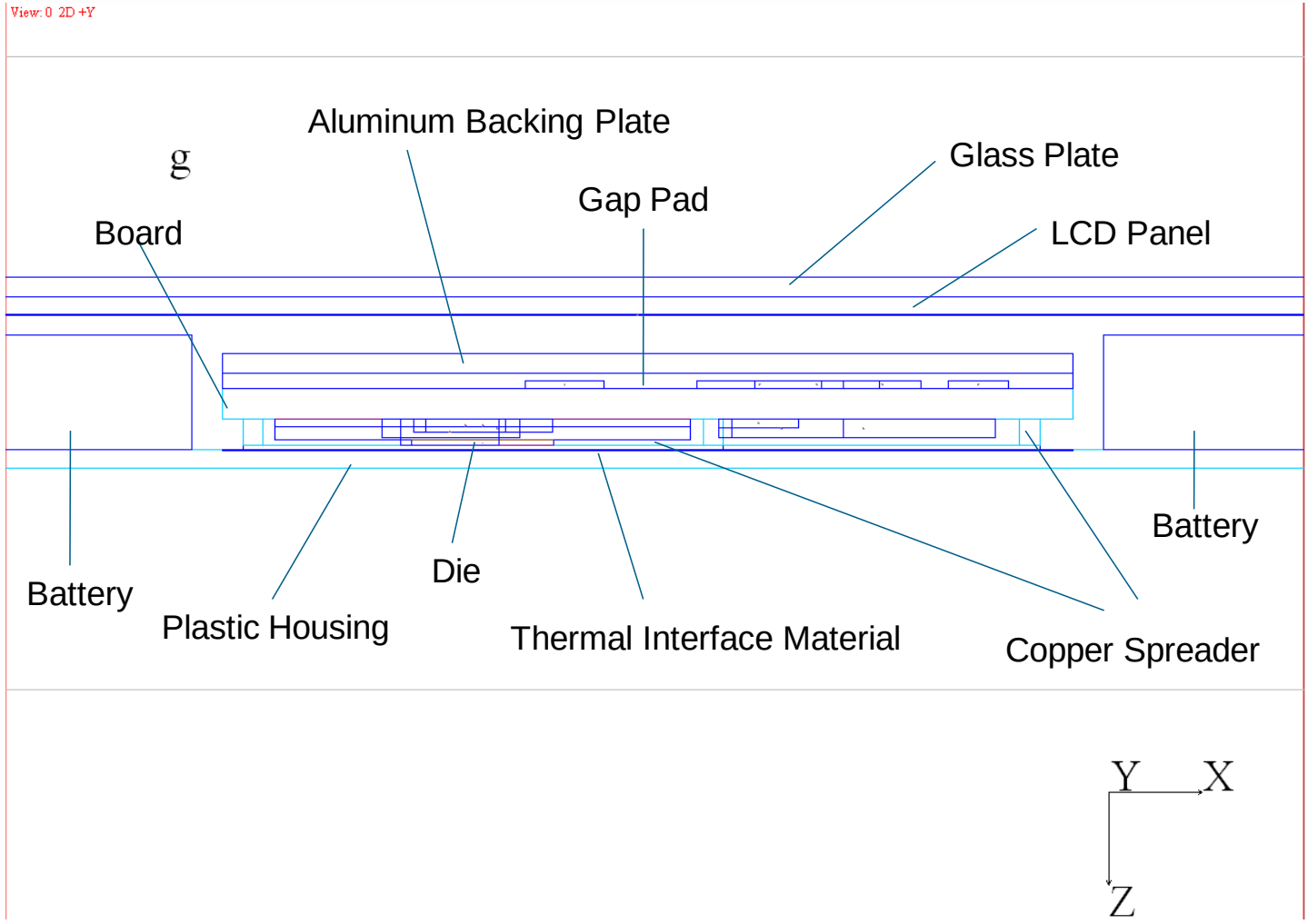
FC-PBGA Thermal Performance

Geometry of Simplified Thermal Model



FC-PBGA Thermal Performance

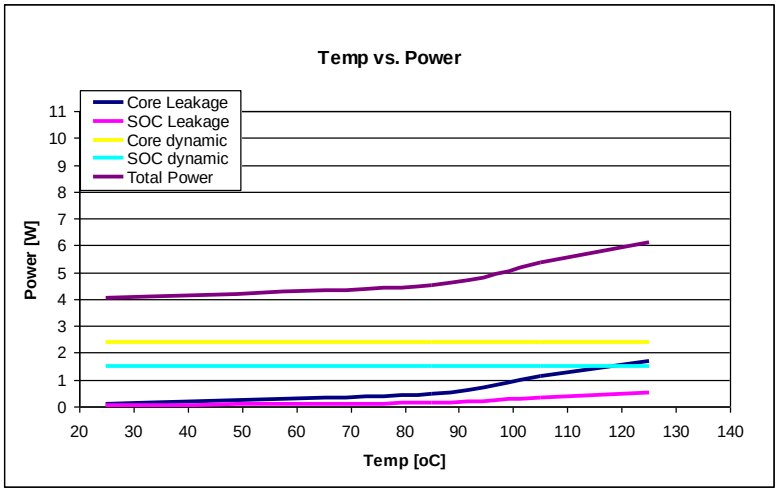
End View



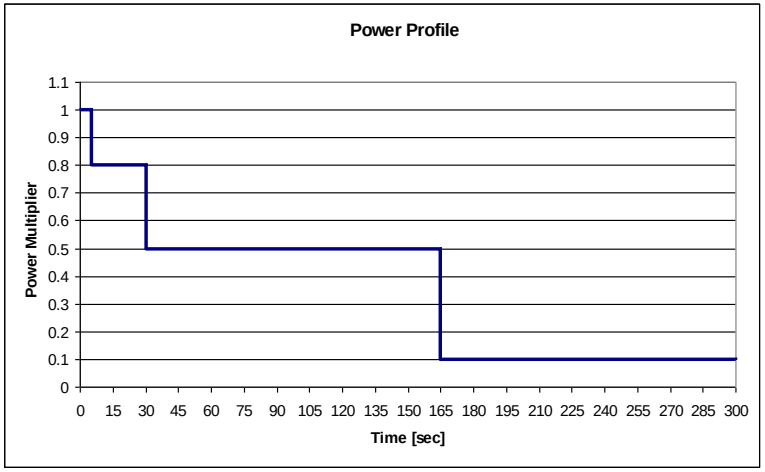
FC-PBGA Thermal Performance

Case 1: 2GHz Configuration Power Cycle (transient profile non-linear source)

Power Vs. Temperature:



Power Cycling Profile:



5 sec at max power
25 sec at of 80% of max power
135 sec at 50% of max power
135 sec at low power (10% of max power) .

Other components:

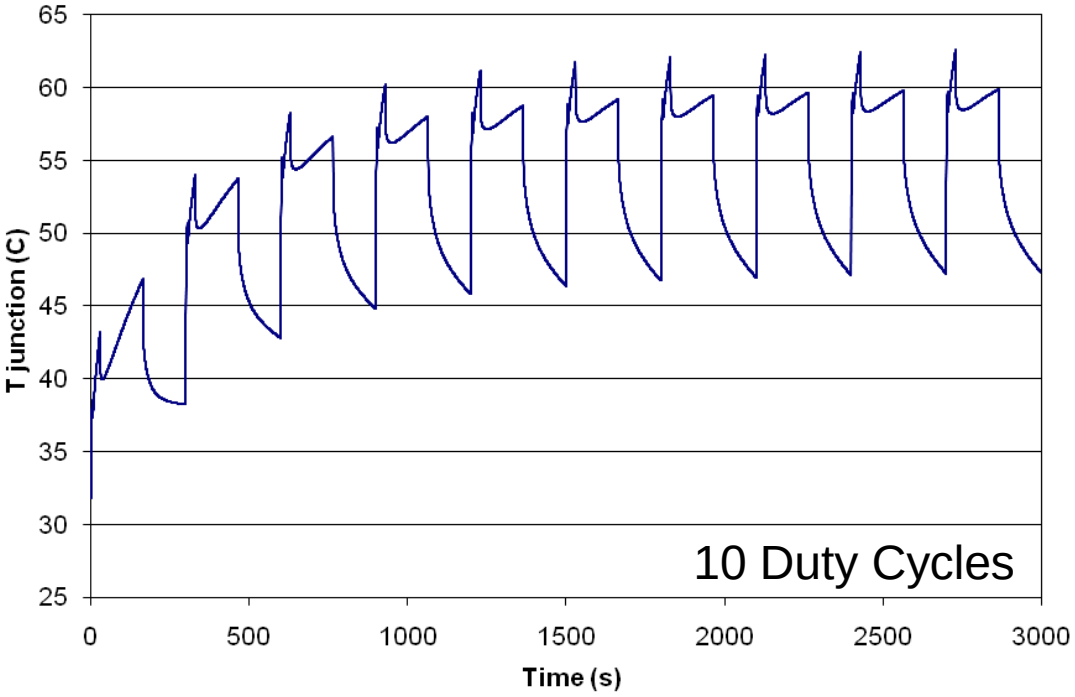
PCB – 0.88W constant (distributed evenly over board components)

LCD – 1W constant

Memory (max power)– 0.65W

FC-PBGA Thermal Performance

Junction Temperature Variation with Time

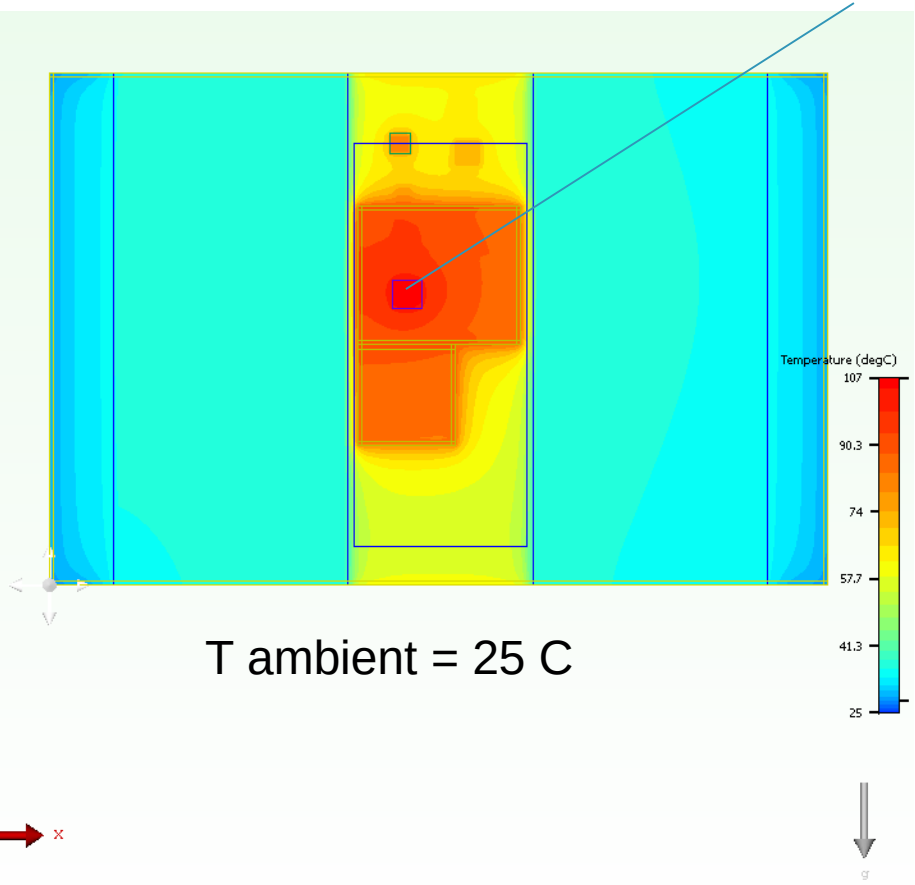


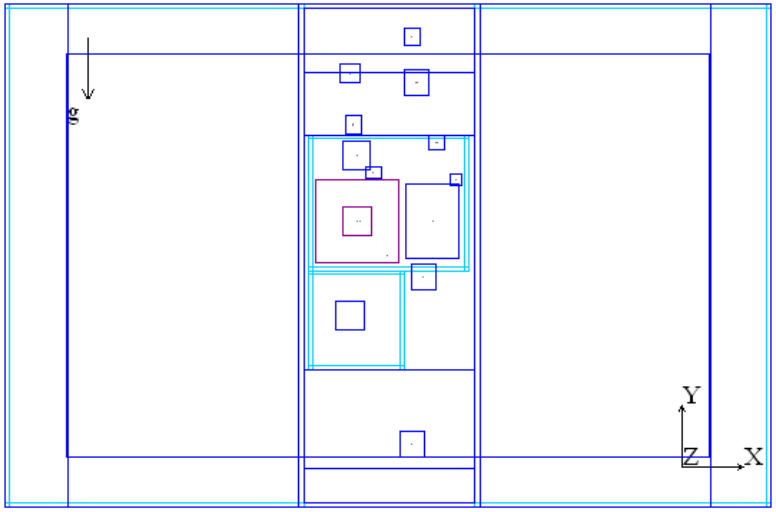
T ambient = 25 C

FC-PBGA Thermal Performance

Temperature Profile, Plane through Die, Steady State Solution

T junction = 106.6 C





T ambient = 25 C

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