

S12ZVM32_1N14N/0P33K

Mask Set Errata



Mask Set Errata for Mask 1N14N/0P33K

Revision History

This report applies to mask 1N14N/0P33K for these products:

- S12ZVM32

Table 1. Mask Specific Information

major_mask_rev_num	1N14N
minor_mask_rev_num	0P33K
label_one	Revised to include alternate mask set 0P33K. No changes to the errata with this revision.

Table 2. Revision History

Revision	Date	Significant Changes
1 November 2023	11/2023	No changes to errata with this revision
9 January 2016	7/2016	Initial Revision

Errata and Information Summary

Table 3. Errata and Information Summary

Erratum ID	Erratum Title
ERR009318	PMF: Glitch visible in PWM asymmetric operation mode

Known Errata

ERR009318: PMF: Glitch visible in PWM asymmetric operation mode

Description

When any of the PWM pairs in the PMF module is operating in asymmetric complementary center-aligned mode, with half cycle reload enabled.

PMF configuration:

- Complementary mode: PMFCFG0_INDEP{A,B,C}=0
- Center aligned outputs: PMFCFG0_EDGE{A,B,C}=0
- Asymmetric mode: PMFICCTL_ICC{A,B,C}=1
- Normal pulse edge control: PMFICCTL_PEC{A,B,C}=0
- Half cycle reload enabled: PMFFQC{A,B,C}_HALF{A,B,C}=1

And any of the following two conditions below (A or B) occur, an unexpected pulse with a width of “dead time” will be visible in the corresponding odd PWM channel output (PWM1,3 or 5)

Condition A.

1a. Setting the odd PWM channel to 0 (PMFVAL{1,3,5}=0) and loaded into the internal buffer (LDOKA=1) before next half cycle start, and

2a. Setting the even PWM channel to 0 (PMFVAL{0,2,4}=0) and loaded into the internal buffer (LDOKA=1) before next full cycle start.

Condition B.

1b. Setting the odd PWM channel to 0 (PMFVAL{1,3,5}=0) and loaded into the internal buffer (LDOKA=1) before next full cycle start, and

2b. Setting the even PWM channel to 0 (PMFVAL{0,2,4}=0) before next full cycle start and loaded into the internal buffer (LDOKA=1) before next full cycle start

Workaround

Set both VAL registers of each complementary pair, PMFVAL{1,3,5} and PMFVAL{0,2,4}, to zero before the next half cycle start to disable the PMF output and correct the unexpected pulse

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