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Ensuring Data Integrity on the i.MX35 EMI

by *Multimedia Applications Division*
Freescale Semiconductor, Inc.
Austin, TX

Typical i.MX35-based applications employ MobileDDR or DDR2 memory as the external SDRAM memory. While writing certain data patterns to memory, a transient pulse may be induced on the DQS[3:0] lines. This transient pulse, if large enough, may appear as valid strobes to some external memory devices, potentially causing data corruption.

This Engineering Bulletin explains the technique required to minimize the size of these transient pulses in i.MX35-based designs to ensure SDRAM data integrity. The following devices are affected by this document:

- PCIMX357CVM5B
- MCIMX353CVM5B
- MCIMX353DVM5B
- MCIMX357CVM5B
- MCIMX357DVM5B
- MCIMX351AVM4B
- MCIMX351AVM5B
- MCIMX355AVM4B
- MCIMX355AVM5B
- MCIMX356AVM4B
- MCIMX356AVM5B

Contents

1 Issue

When an silicon revision TO1.0 or TO2.0 i.MX35 device writes to external memory, a transient may be observed on the DQS[3:0] traces during the transition of the SD[31:0] signals from HIGH to LOW or from LOW to HIGH. At times, the amplitude of the transient may exceed the logic threshold limits of the external memory device(s) connected to the i.MX35. When this occurs, there is a possibility that the transient may be seen by the external memory device(s) as an extra clock pulse that may corrupt the data written into the memory device.

Figure 1 shows a scope plot of the transients on the DQS0 signal. The transients were captured as two words 0x00000000 and 0xFFFFFFFF were written sequentially to the bus on the first two transitions of the DQS0 signal (yellow trace). The SD31 data signal is included in the plot (purple trace). Only two words were written to the bus, but due to the internal operation of the EMI block, the same two words are alternately written to the bus through the remaining six words of the 8-word burst. This data sequence stimulates the worst case transient response from the silicon revision TO2.0 i.MX35 device.

Figure 1 was generated using MDDR mode with HIGH drive strength level for all signals on an i.MX35 PDK CPU card with mDDR memory. This drive strength configuration was used because it is the default recommendation configuration for an mDDR-based system.

Figure 1. Representative Scope Trace of Transient During a Write Cycle

The first two transients corresponding to the two written words are marked in Figure 1 with green arrows. The horizontal cursor marks the highest positive-going transient in the burst. In this plot, the transient magnitude is 1.029 V, which exceeds the maximum VIL (0.3 × NVCC_EMI) for mDDR memory. Although the thresholds are different for DDR2 memory (dynamic limits relative to Vref), errors may still

be induced by these transients. During investigation, transient induced errors were stimulated with either type of memory, mDDR or DDR2.

2 Root Cause

The root cause of the transients lies in the following factors:

- Physical interconnection between the die and the package substrate
- Routing of the DQSx signals to the balls
- Proximity of those balls to the DDR power supply lines

The transients are also affected by the drive strength configuration programmed into the IOMUX registers for the DDR pads.

2.1 Inductive Coupling: Wire Bonds

In order to accommodate the density of interconnects on the i.MX35 device, two rows of bond pads are required on each edge of the die as well as on the package substrate. A partial diagram of this inner and outer bond wire configuration is shown in Figure 2. The shorter (green) bond wires are placed first during manufacturing and the longer (gray) bond wires are placed subsequently.

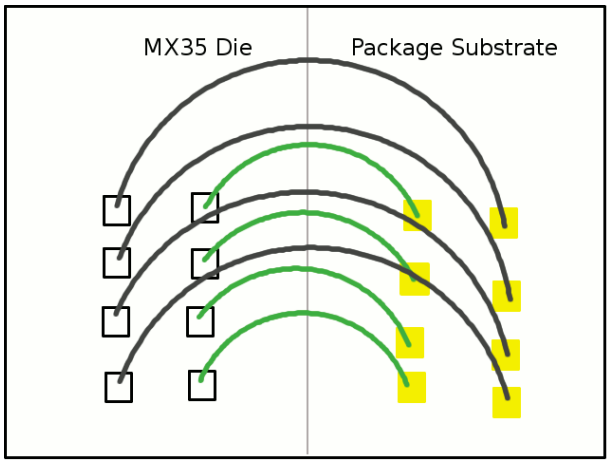

Figure 2. Partial Wire Bond Diagram Showing Inner and Outer Wire Bonds

The physical configuration of the two rows of bond wires is similar to a cross-section of the windings in a transformer. As such, coupling occurs due to the proximity of the bond wires to each other. As a result, currents can be induced in adjacent bond wires when a significant quantity of the external memory interface signals simultaneously transition in the same direction. This is not generally an issue for signals that transition in sync with each other (where the edges are aligned), but the DQSx signals are data strobes that do not transition when the data lines are transitioning and vice versa.

The transients on the DQSx signals observed in the TO1.0 and TO2.0 silicon revisions of the i.MX35 device arise as the cooperative result of the skewed transition edges along with the fact that these silicon revisions use the longer, more inductive, outer set of bond wires for all the DQSx signals.

2.2 Return Path: Sub-Optimal Ball Map and Substrate Routing

Effective high speed design practice dictates that the return path closely follow the signal path, otherwise bounce may be introduced into a signal. Figure 3 shows a partial ball map of the i.MX35 device and shows the relative distance between the DQSx signals (yellow) and the concentration of power supply balls (gray). The routing on the substrate of the signals between the bond pads adjacent to the i.MX35 die and the ball pads coupled with the distance to the power supply balls in the center of the package is not ideal. This unfavorable routing makes a significant contribution to the transients observed on the DQSx signals.

OLD	7	8	9	10	11	12	13	14	15	16	17
A	SD30	SD27	SD24	DQS2	SD21	SD18	DQS1	SD14	SD10	SD9	SD6
B	SD31	SD28	SD26	SD23	SD20	SD19	SD15	SD13	SD11	SD7	DQS0
C	DQS3	SD29	SD25	SD22	SD17	SD16	SD12	SD8	SD5	SD3	SD0
D	A1	A24	A22	A20	A19	A17	A16	A14	A15	DQM2	DQM1
E	A2	A25	A23	A21	A18	SDCLK	SDCLKB	BCLK	RAS	CAS	SDCKE1
F	VDD7	VDD7	VDD7	NVCC_EMI1	NVCC_EMI1	VDD7	NVCC_EMI2	NVCC_EMI2	A10	EB1	CS0
G	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI2	VDD6	NVCC_EMI3	SDWE	LD3	LD2
H	NVCC_NFC	GND	NVCC_EMI1	GND	GND	GND	GND	NVCC_LCDC	VDD5	LD5	LD8

Figure 3. Partial i.MX35 Ball Map Showing DQSx Signals

2.3 Drive Strength Configuration

The observed DQSx transients are proportional to the drive strengths configured by software in the IOMUX for the DDR pads. Therefore, with all other factors being equal, the stronger the drive strength, the larger the observed transient.

3 Other Concerns: i.MX35 Read Operation

Given that the factors from Section 2, “Root Cause,” may interact adversely during i.MX35 write operations, the question of whether these factors also affect read operations naturally arises. This question was addressed during the investigation into the root cause of the transient behavior of the DQSx signals.

Unlike the write operation, the bus protocol dictates that when an external memory device is writing data to the i.MX35, the data and DQSx signals are edge aligned. Internal to the i.MX35, the edges of DQSx and the data lines are shifted relative to each other. As such, any transients that may be induced on the DQSx lines by the interactions described in Section 2, “Root Cause,” are superimposed on the edge.

Tests were specifically conducted that programmed the drive strength of the external memory device to all possible levels (for example, full, half and quarter strength) while various data patterns were read back by the i.MX35. The temperature and operating voltage were also varied. In all cases, no errors were induced during the read cycle. The edge alignment of the data and DQSx lines during read accesses eliminates the adverse cooperation of the factors described in Section 2, “Root Cause.”

4 Solutions and Validation

There are two recommended solutions for addressing the DQSx transient issue on the i.MX35 device:

- Work around by adding transient suppression RC filters to existing TO2.0 i.MX35 designs
- Migrate to the TO2.1 silicon revision of the i.MX35

4.1 Work Around: TO2.0 Existing Designs

For existing, qualified designs using the TO2.0 silicon revision, the addition of transient suppressing RC filters to all four DQSx signals as well as the SDCLKD and SDCLK_B lines is recommended. These filters consist of a series resistor with a capacitor placed as closely as possible to the memory device. The filtering scheme used on the i.MX35 mDDR CPU card is shown in a partial schematic in Figure 4.

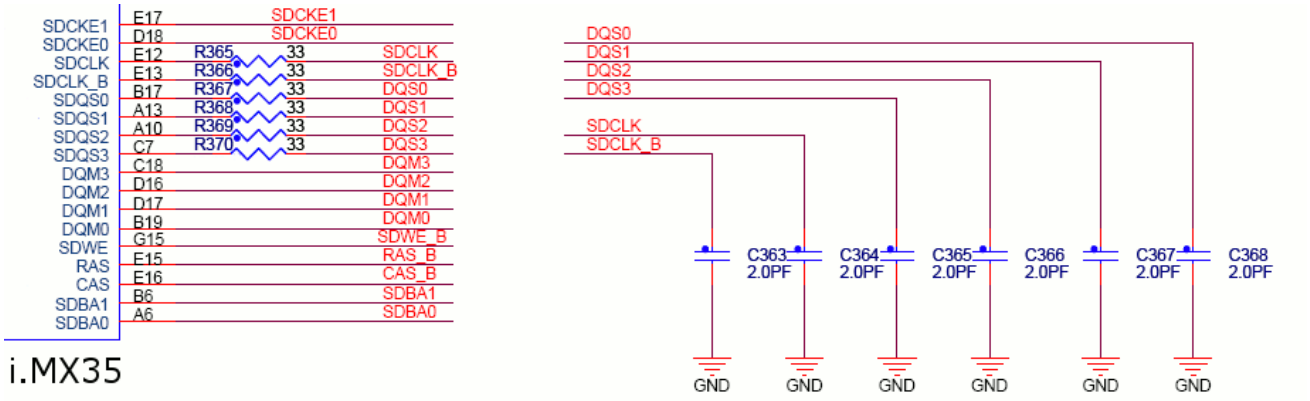

Figure 4. Partial Schematic of Filters Placed on DQS[0:3], SDCLK, and SDCLK_B Signals

The values for the series resistor and the terminating capacitor should be the same for all six signals. The size of the resistor and capacitor requires an iterative procedure where the parameters of the i.MX35 device and package, the external memory device and the application board are all entered into a complex model for the transient behavior. The process is iterative because the selection of the component values requires balancing all system requirements for bus timing, threshold levels, operating voltage and temperature of each component in the system.

For the i.MX35 mDDR CPU card, the component values chosen were a series resistance of 33 Ω and a termination capacitance of 2 pF. The RC filters were added to the SDCLK and SDCLK_B clock lines to keep any skew between the DQSx signals and these clock lines to a minimum.

The addition of RC filtering addresses the hardware side of the issue. On the software/firmware side, the best performance is obtained when the drive strength of the data lines is set slightly lower than the drive strength of the rest of the EMI signals. It is recommended to use SDRAM/MAX for all the data lines and

MDDR/HIGH for the remainder of the EMI signals. The drive strength parameters are used in the simulations for determining the RC component values, so these parameters are also obtained iteratively.

The drive mode specified in the IOMUX registers is used by the internal circuitry of the i.MX35 device and does not affect the bus protocol. Table 1 shows the relative drive strength combinations that may be selected for any of the DDR-type pads of the IOMUX, sorted in order of increasing drive strength.

Table 1. Drive Mode and Strength

Mode	Strength
SDRAM	Standard
SDRAM	High
MDDR	Standard
SDRAM	Max
MDDR	High
MDDR	Max
DDR2	–

Figure 5 shows a scope trace for a i.MX35 TO2.0 mDDR CPU card with the RC filter (33 Ω and 2 pF) implemented. The conditions for Figure 5 are identical to those of Figure 1, with the exception that Figure 5 uses the drive strength configuration of SDRAM/MAX for the data lines and MDDR/HIGH for the remainder of the EMI signals.

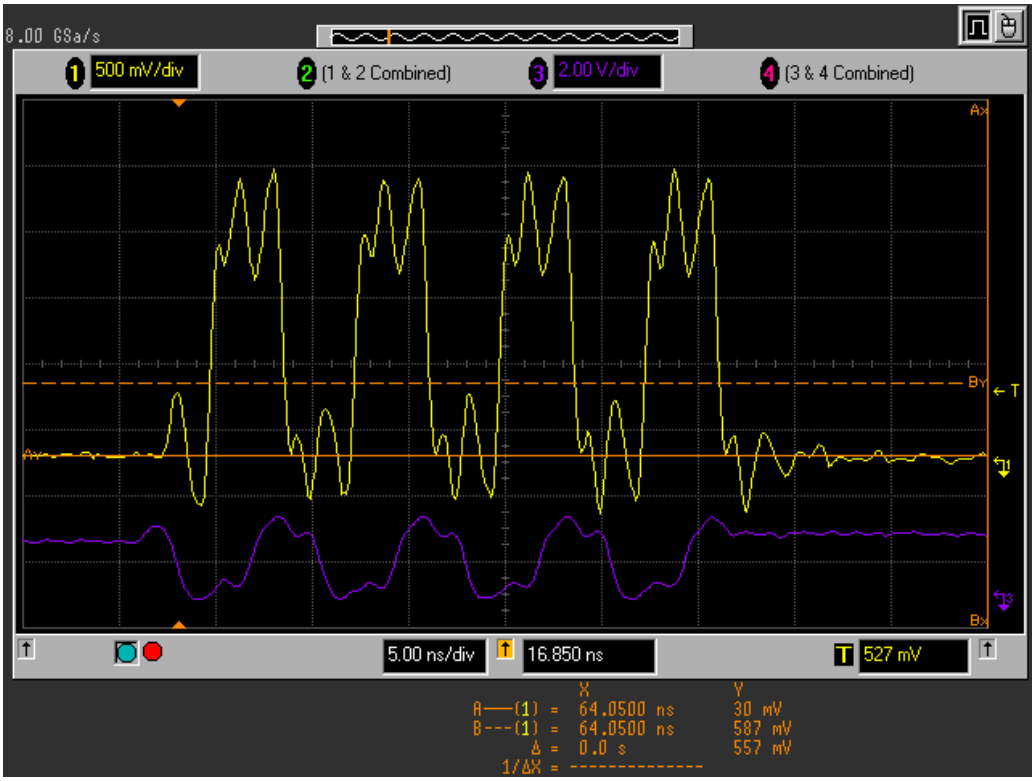

Figure 5. Scope Capture of Filtered DQS0 Signal

The transient level in Figure 5 is reduced by about half. The waveform easily meets DDR2 threshold requirements. For mDDR, the maximum VIL permitted is 0.3 × NVCC_EMI, which for a value of 1.8 V, VIL would be equal to 0.54 V. For this board, slightly more resistance can be used to reduce the maximum transient level even further.

4.2 Migrate to New Ball Map: TO2.1, New and Re-Designs

The preferred solution to the DQSx transient issue is to use the i.MX35 TO2.1 silicon revision, which has greatly improved transient performance and requires no external RC filtering.

The improvements made to the i.MX35 in revision TO2.1 are as follows:

- DQSx signals are bonded with the shorter, inner row of bond wires
- Substrate routing between the bond and ball pads is greatly improved
- Twenty three signals are shifted to move the DQSx signals closer to the power supply balls

For the first improvement, the die of the i.MX35 was modified such that the DQSx signals could be bonded on either the inner or outer pad ring of the die to allow the same die to be packaged into either ball map of the device. The advantage of this modification was that existing die probing hardware can continue to be used while greatly reducing the length and inductance of the bond wires that connect the DQSx bond pads to the substrate in the new package. As a result, the inductive coupling effect is greatly reduced.

The last two improvements work together. Moving the DQSx balls closer to the power supply region and improving the substrate routing, greatly reduces the return path both on the application board as well as on the i.MX35 package substrate. Figure 6 shows a partial ball map of the revised package where the 23 signals that were moved relative to TO2.0 are highlighted in pink. The arrows show the location from where each signal was moved.

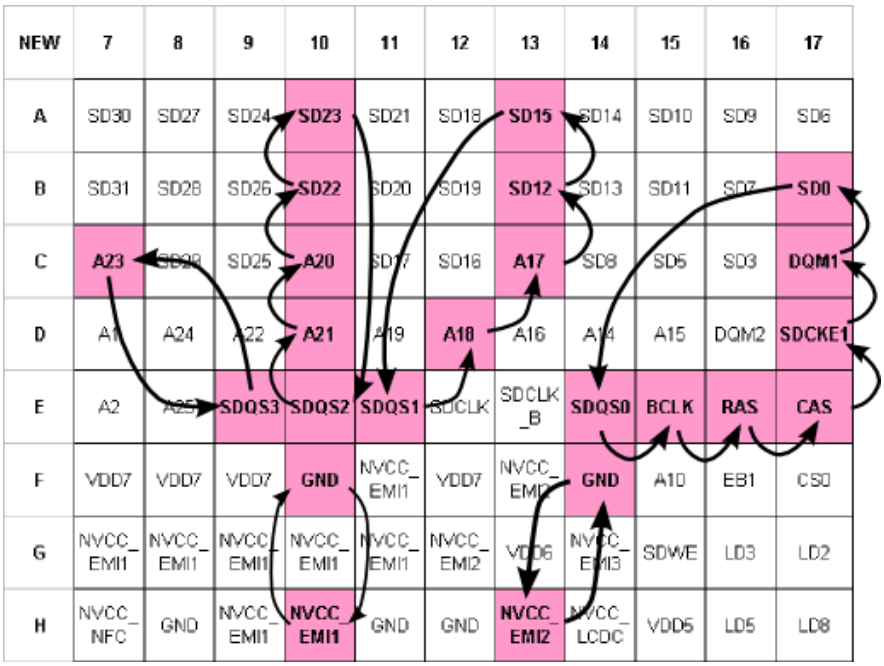

Figure 6. Partial Ball Map for i.MX35 TO2.1

Table 2 shows the different ball assignments for the TO2.0 and TO2.1 silicon revisions.

Table 2. Signal Differences Between TO2.0 and TO2.1

Ball	Old Pinout (TO2.0) Signal	New Pinout (TO2.1) Signal
A10	DQS2	SD23
A13	DQS1	SD15
B10	SD23	SD22
B13	SD15	SD12
B17	DQS0	SD0
C7	DQS3	A23
C10	SD22	A20
C13	SD12	A17
C17	SD0	DQM1
D10	A20	A21
D12	A17	A18
D17	DQM1	SDCKE1
E9	A23	DQS3
E10	A21	DQS2
E11	A18	DQS1
E14	BCLK	DQS0
E15	RAS	BCLK
E16	CAS	RAS
E17	SDCKE1	CAS
F10	NVCC_EMI1	GND
F14	NVCC_EMI2	GND
H10	GND	NVCC_EMI1
H13	GND	NVCC_EMI2

In Figure 7, the DQSx signals are highlighted in yellow. In comparison to Figure 3, the DQSx signals are much closer to the power supply area, and no further away than a single ball to a ground ball.

The i.MX35 mDDR CPU card was re-laid out for the to TO2.1 silicon revision ball map with minimal changes to the existing filtered mDDR board layout. Figure 8 shows an oscilloscope capture of the DQS0 signal from the revised TO2.1 mDDR CPU card with the drive strength set to SDRAM/MAX for the data

lines and MDDR/HIGH for the remainder of the EMI signals. The transient level is reduced by half again as much as the filtered TO2.0 DQS0 signal seen in Figure 5.

NEW	7	8	9	10	11	12	13	14	15	16	17
A	SD30	SD27	SD24	**SD23**	SD21	SD18	**SD15**	SD14	SD10	SD9	SD6
B	SD31	SD28	SD26	**SD22**	SD20	SD19	**SD12**	SD13	SD11	SD7	**SD0**
C	**A23**	SD29	SD25	**A20**	SD17	SD16	**A17**	SD8	SD5	SD3	**DQM1**
D	A1	A24	A22	**A21**	A19	**A18**	A16	A14	A15	DQM2	**SDCKE1**
E	A2	A25	**SDQS3**	**SDQS2**	**SDQS1**	SDCLK	SDCLK_B	**SDQS0**	**BCLK**	**RAS**	**CAS**
F	VDD7	VDD7	VDD7	**GND**	NVCC_EMI1	VDD7	NVCC_EMI2	**GND**	A10	EB1	CS0
G	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI1	NVCC_EMI2	VDD6	NVCC_EMI3	SDWE	LD3	LD2
H	NVCC_NFC	GND	NVCC_EMI1	**NVCC_EMI1**	GND	GND	**NVCC_EMI2**	NVCC_LCDC	VDD5	LD5	LD8

Figure 7. Partial Ball Map Showing the Proximity of the DQSx Signals to GND

Figure 9 is included to emphasize the fact that the most significant contributors to the root cause of the transient were correctly identified and resolved by shortening the bond wires, improving the substrate routing and revising the ball map. Even with all the drive strengths set to DDR2, the maximum

configurable drive strength, the transient level in Figure 9 is still about half of that seen in Figure 1, which used MDDR/HIGH for all the signals.

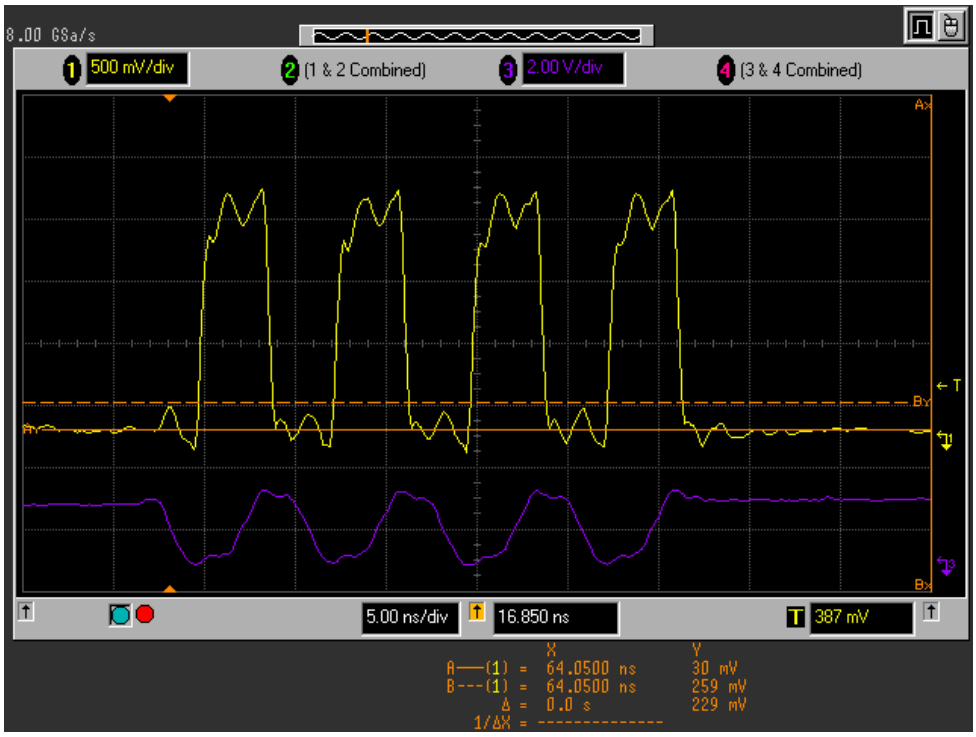

Figure 8. Scope Capture of DQS0 with T02.1 Silicon

Figure 9. Scope Capture of DQS0 with DDR2 Drive Strength

5 Conclusions

The major contributors to the transients observed on DQS[3:0] of the i.MX35 revision TO2.0 silicon were identified as the inductive coupling with the adjacent bond wires of the data lines working with an un-optimized ball map and package substrate routing.

To correct this issue, the i.MX35 die was minimally modified to create parallel bond pads for the DQSx signals so that they could be bonded with the shorter length bond wires. This had the advantage of leveraging existing probe hardware while allowing the same die to go into either package (TO2.0 or TO2.1).

The ball map was revised to bring the DQSx signals closer to the power supply return path because simulations conducted during the investigation showed that the shorter bond wires alone would not result in enough reduction of the transients. The number of signals shifted was kept to the minimum required to move the DQSx signals to be adjacent to the power supply balls in the center of the package.

Figure 8 and Figure 9 clearly show that the most significant contributors to the transient have been addressed.

6 Recommendations

The preferred solution to the transient issue on the DQSx signals on the i.MX35 revision TO2.0 is to migrate to the revised ball map device, TO2.1. The performance is greatly improved and requires no external support circuitry.

For existing applications that use TO2.0 and are not able to migrate, RC filters should be added to the four DQSx signals as well as the SDCLK and SDCLK_B signals. The resistor and capacitor component values depend on the application board layout and specific memory bus configuration.

7 Revision History

Table 3 provides a revision history for this application note.

Table 3. Document Revision History

Rev. Number	Date	Substantive Change(s)
2	12/2009	Entire document was significantly updated to include information about the new T02.1 silicon revision
1	09/2009	• Added filter placement information. • Added plots of transient with and without recommended filtering.
0	08/2009	Initial release.

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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800 441-2447 or
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Fax: +1-303-675-2150
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