

# 88W8987\_SDS

## 2.4/5 GHz Dual-band 1x1 Wi-Fi 5 (802.11ac) and Bluetooth 5.2 Solution

Rev. 6 — 2 December 2022

Product short data sheet

### 1 Product overview

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The 88W8987 is a highly integrated Wi-Fi (2.4/5 GHz) and Bluetooth single-chip solution, specifically designed to support the speed, reliability, and quality requirements of next generation Very High Throughput (VHT) products.

The System-on-Chip (SoC) provides both simultaneous and independent operation of the following:

- IEEE 802.11ac (Wave 2), 1x1 with data rates up to MCS9 (433 Mbit/s)
- Bluetooth 5.2 (includes Bluetooth Low Energy (LE))

The SoC also provides:

- Bluetooth Classic and Bluetooth LE dual (Smart Ready) operation
- Wi-Fi indoor location positioning (802.11mc)

For security, the device supports high performance 802.11i security standards through implementation of the Advanced Encryption Standard (AES)/Counter Mode CBC-MAC Protocol (CCMP), AES/Galois/Counter Mode Protocol (GCMP), AES/Cipher-Based Message Authentication Code (CMAC), and WLAN Authentication and Privacy Infrastructure (WAPI) security mechanisms.

For video, voice, and multimedia applications, 802.11e Quality of Service (QoS) is supported. The device also supports 802.11h Dynamic Frequency Selection (DFS) for detecting radar pulses when operating in the 5 GHz range.

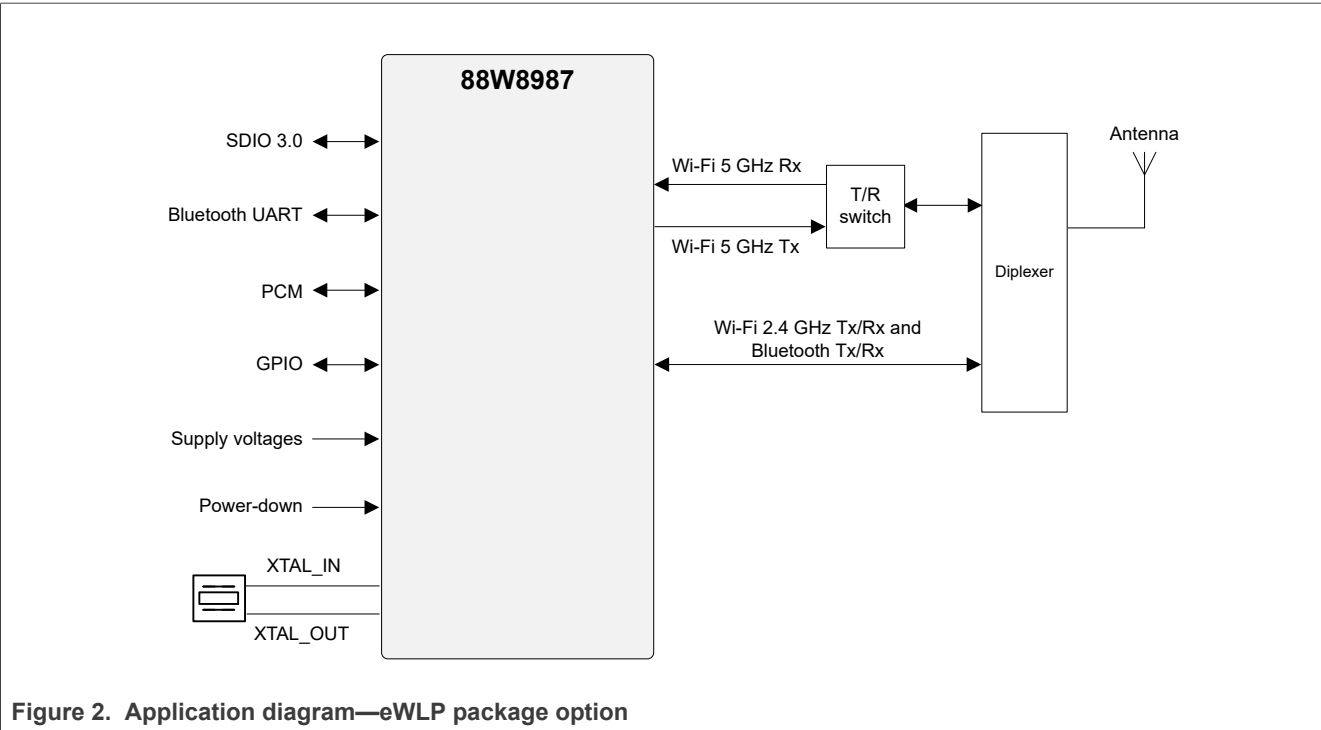
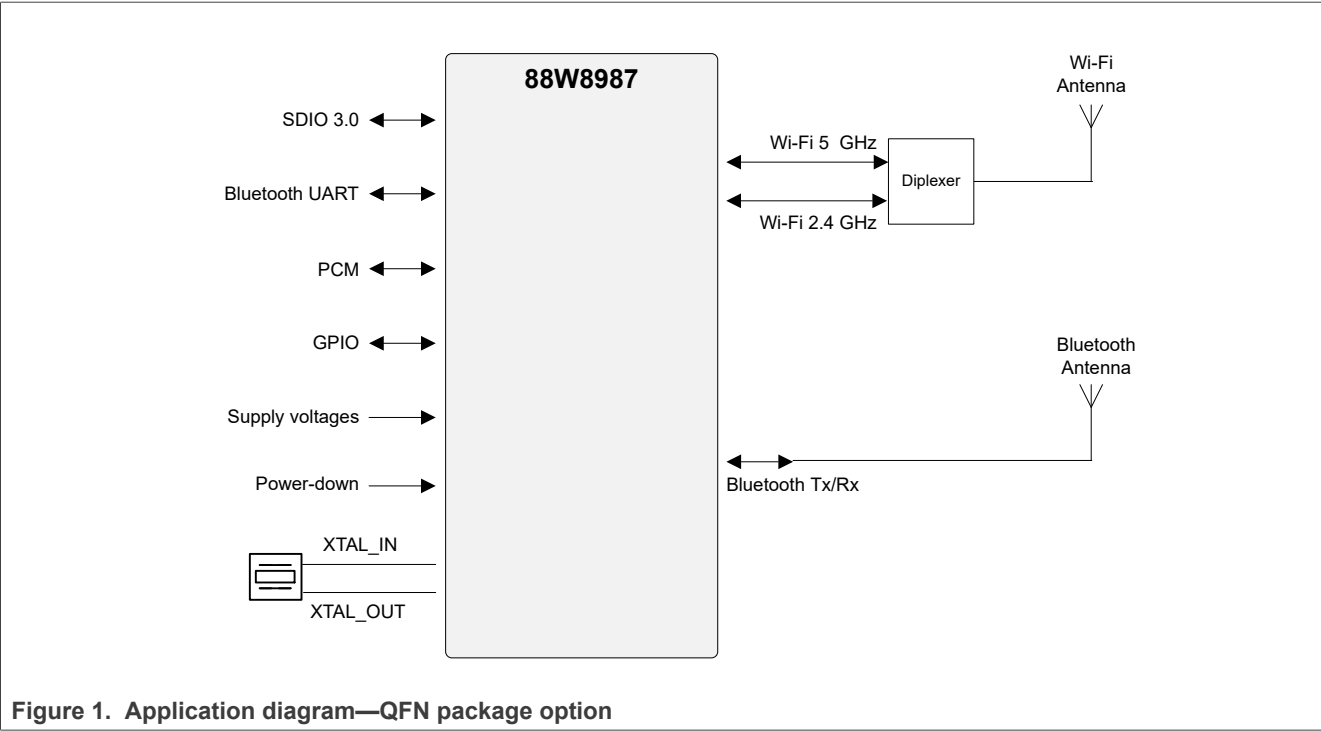
Host interfaces include SDIO 3.0 and high-speed UART interfaces for connecting Wi-Fi and Bluetooth technologies to the host processor.

The device is designed with two front-end configurations to accommodate Wi-Fi and Bluetooth on either separate or shared paths:

- 2-antenna configuration—1x1 Wi-Fi and Bluetooth on separate paths (QFN)
- 1-antenna configuration—1x1 Wi-Fi and Bluetooth on shared paths (eWLP)

The following figures show the application diagrams for each package option.





## 1.1 Applications

- Wi-Fi and Bluetooth enabled smart phones and tablets
- Personal computing systems including notebooks and ultrabooks
- Wireless home audio and video entertainment systems
- Mobile routers and Internet of Things (IoT) gateways

## 1.2 Wi-Fi key features

- Support 802.11ac/n/a/g/b
- Dual band: 2.4 GHz and 5 GHz
- Up to MCS9 data rates
- 20/40/80 MHz channel bandwidth
- Security: AES, WAPI

## 1.3 Bluetooth key features

- Bluetooth 5.2 support
- PCM audio interface
- Security: AES

## 1.4 Host interfaces

Wi-Fi and Bluetooth host interface options

| Wi-Fi    | Bluetooth |
|----------|-----------|
| SDIO 3.0 | UART      |
| SDIO 3.0 | SDIO 3.0  |

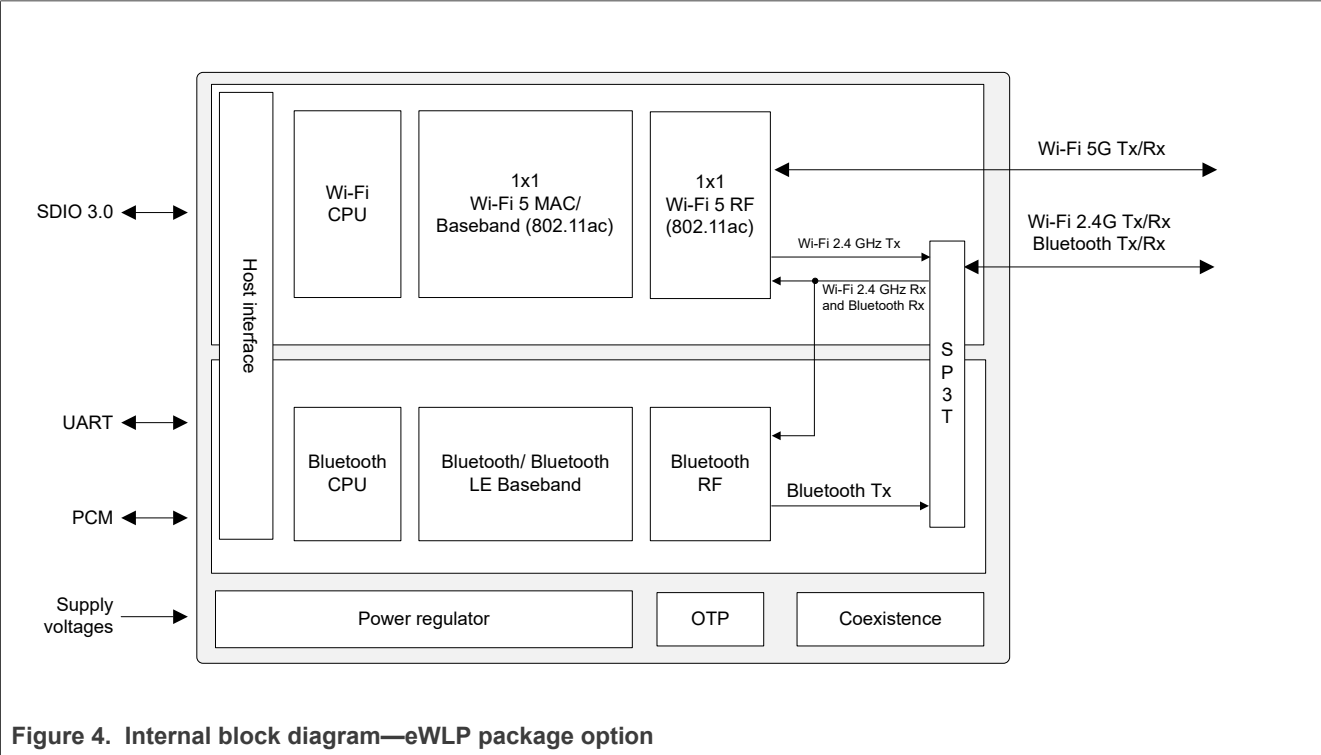
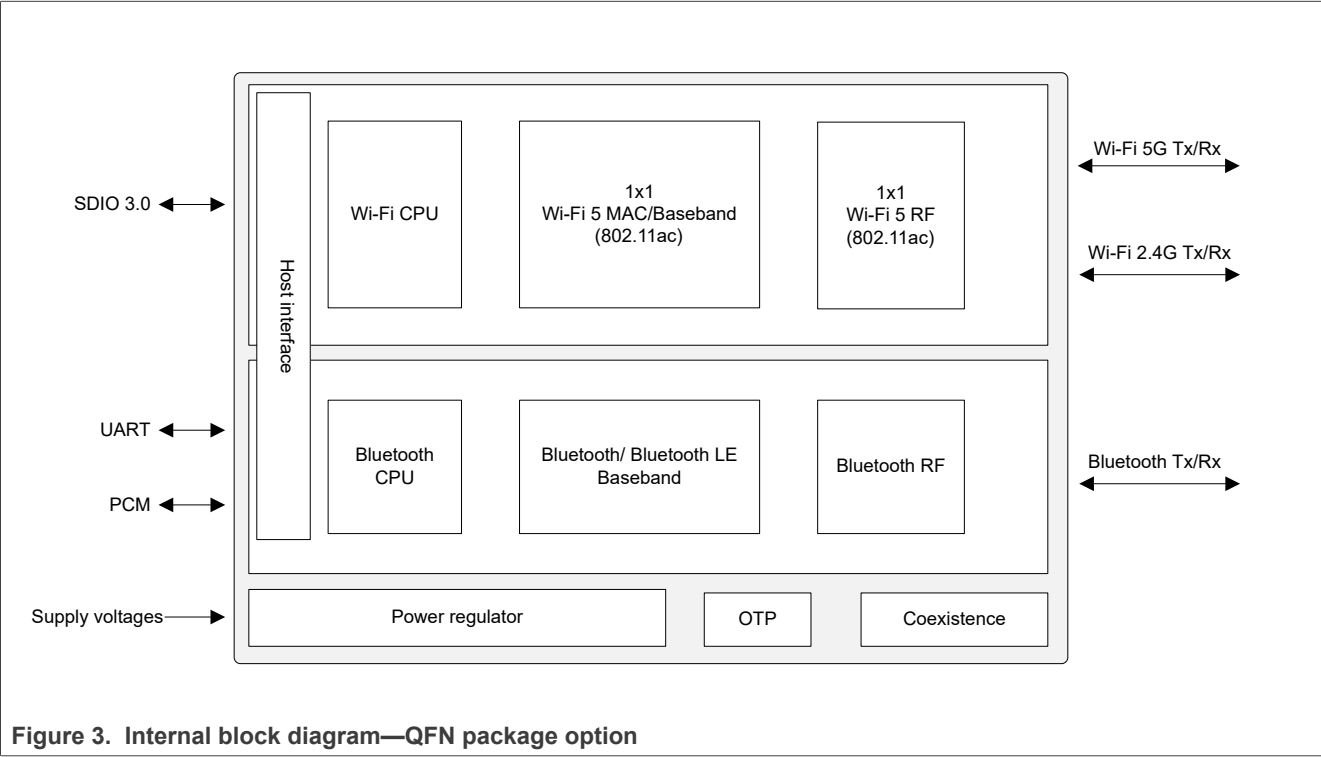
## 1.5 Operating characteristics

- Supply voltage: 2.2V, 1.8V, and 1.1V
- Operating temperature
  - Extended: -30 to 85°C
  - Industrial: -40 to 85°C

## 1.6 General features

- Package options
  - 68-pin 8x8 mm QFN with wettable flanks
  - 83-bump 4.6x4.2 mm eWLP
- Power management
  - Low power dissipation
  - Optional lower power operation with external sleep clock
  - Sleep and standby modes for low-power operation
- Independent ARM-based Wi-Fi and Bluetooth CPUs
- Supports reference clock signal from external crystal or external crystal oscillator
- Memory
  - Internal SRAM
  - Boot ROM
  - One Time Programmable (OTP) memory to store the MAC address and calibration data
- Peripheral interfaces
  - GPIO interface (up to 21)

1.7 Internal block diagram



## 2 Ordering information

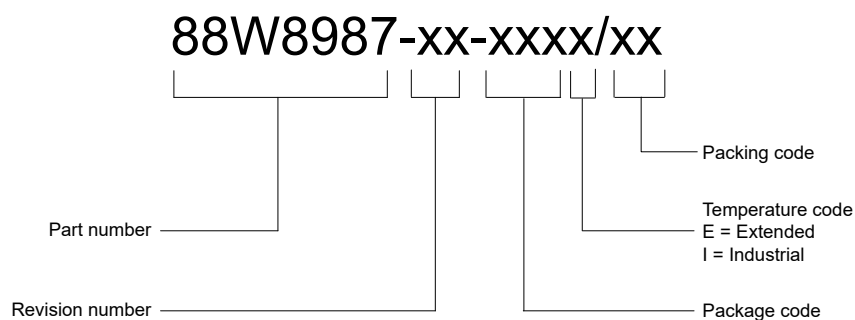


Figure 5. Part numbering scheme

Table 1. Part order codes

| Part order code    | Package type                                              | Packing       |
|--------------------|-----------------------------------------------------------|---------------|
| 88W8987-A2-NYEE/AK | 68-pin HVQFN - 8 x 8 x 0.85 mm, with 0.4 mm pitch         | Tray          |
| 88W8987-A2-NYEE/AZ | 68-pin HVQFN - 8 x 8 x 0.85 mm, with 0.4 mm pitch         | Tape and reel |
| 88W8987-A2-NYEI/AK | 68-pin HVQFN - 8 x 8 x 0.85 mm, with 0.4 mm pitch         | Tray          |
| 88W8987-A2-NYEI/AZ | 68-pin HVQFN - 8 x 8 x 0.85 mm, with 0.4 mm pitch         | Tape and reel |
| 88W8987-A2-EAHE/AZ | 83-terminal eWLP - 4.6 x 4.2 x 0.75 mm, with 0.4 mm pitch | Tape and reel |

### 3 Wi-Fi subsystem

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#### 3.1 IEEE 802.11 standards

- 802.11 data rates of 1 and 2 Mbit/s
- 802.11b data rates of 5.5 and 11 Mbit/s
- 802.11a/g data rates 6, 9, 12, 18, 24, 36, 48, and 54 Mbit/s for multimedia content transmission
- 802.11g/b performance enhancements
- 802.11ac / 802.11n with maximum data rates up to 86.7 Mbit/s (20 MHz channel), 200 Mbit/s (40 MHz channel), 433 Mbit/s (80 MHz channel)
- 802.11d international roaming
- 802.11e quality of service
- 802.11h transmit power control
- 802.11h DFS radar pulse detection
- 802.11i enhanced security
- 802.11k radio resource measurement
- 802.11mc precise indoor location positioning
- 802.11n block acknowledgment extension
- 802.11r fast hand-off for AP roaming
- 802.11u Hotspot 2.0 (STA mode only)
- 802.11v TIM frame transmission/reception
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode

### 3.2 Wi-Fi MAC

- Simultaneous peer-to-peer and Infrastructure Modes
- RTS/CTS for operation under DCF
- Hardware filtering of 32 multicast addresses and duplicate frame detection for up to 32 unicast addresses
- On-chip Tx and Rx FIFO for maximum throughput
- Open System and Shared Key Authentication services
- A-MPDU Rx (de-aggregation) and Tx (aggregation) (supports 802.11ac single-MPDU A-MPDU)
- 20/40/80 MHz coexistence
- Reduced Inter-Frame Spacing (RIFS) receive
- Management information base counters
- Radio resource measurement counters
- Quality of service queues
- Block acknowledgment extension
- Dynamic frequency selection
- Beamforming
  - 802.11ac Explicit Beamformee, supports immediate feedback generation using 802.11ac compressed steering matrix feedback
  - 802.11ac Multi-User Beamformee
  - 802.11n Explicit Beamformee, supports immediate feedback generation using uncompress and compress steering matrix or delayed feedback of all feedback types
- TIM frame transmission/reception
- Multiple-BSS/Station
- Transmit rate adaptation
- Transmit power control
- Long and short preamble generation on a frame-by-frame basis for 802.11b frames
- Mobile hotspot

### 3.3 Wi-Fi baseband

- 802.11ac (on-chip RF radio)
- Backward compatibility with legacy 802.11n/a/g/b technology
- Simultaneous Wi-Fi and Bluetooth receive in single-antenna mode (eWLP only)
- PHY data rates up to 433 Mbit/s
- 20 MHz bandwidth/channel, 40 MHz bandwidth/channel, upper/lower 20 MHz packets in 40 MHz channel, 20 MHz duplicate legacy packets in 40 MHz channel mode operation
- 80 MHz bandwidth/channel, 4 positions of 20 MHz packets in 80 MHz channel, upper/lower 40 MHz packets in 80 MHz channel, 20 MHz quadruplicate legacy packets in 80 MHz channel mode operation
- Modulation and Coding Scheme (MCS)
  - 802.11ac—MCS 0~9 Nsts = 1
  - 802.11n—MCS 0~7 and MCS 32 (duplicate 6 Mbit/s)
- Dynamic frequency selection (radar detection)
  - Enhanced radar detection for long and short pulse radar
  - Enhanced AGC scheme for DFS channel
  - Japan DFS requirements for W53 and W56 frequency bands
- Radio resource measurement
- Optional 802.11ac and 802.11n features:
  - 20/40/80 MHz coexistence with middle-packet detection (GI detection) for enhanced CCA
  - 1 spatial stream STBC reception
  - LDPC transmission and reception for both 802.11n and 802.11ac
  - 256 QAM (MCS 8, 9) modulation, optional support for 802.11ac MCS 9 in 20 MHz using LDPC
  - Short guard interval
  - RIFS on receive path for 802.11n packets
  - 802.11n greenfield Tx/Rx
  - Explicit beamformee support
  - 802.11ac multi-user beamformee
  - MU-PPDUs (receive)
- Wi-Fi indoor locationing (802.11mc)
- Power save features

### 3.4 Wi-Fi radio

- Integrated direct-conversion radio
- 20, 40, and 80 MHz channel bandwidths
- Shared Wi-Fi/Bluetooth receive input scheme for 2.4 GHz band (eWLP only)

#### Wi-Fi Rx path

- Direct conversion architecture eliminates need for external SAW filter
- On-chip gain selectable LNA with optimized noise figure and power consumption
- High dynamic range AGC function in receive mode

#### Wi-Fi Tx path

- Internal PA with power control
- Optimized Tx gain distribution for linearity and noise performance

#### Wi-Fi local oscillator

- Fractional-N for multiple reference clock support
- Fine channel step

### 3.5 Wi-Fi encryption

- Advanced Encryption Standard (AES) / Counter-Mode/CBC-MAC Protocol (CCMP)
- Advanced Encryption Standard (AES) / Cipher-Based Message Authentication Code (CMAC)
- Advanced Encryption Standard (AES) / Galois/Counter Mode Protocol (GCMP)
- WLAN Authentication and Privacy Infrastructure (WAPI)

### 3.6 Wi-Fi host interfaces

- SDIO 3.0 device interface (4-bit SDIO and 1-bit SDIO) transfer modes at full clock range up to 208 MHz

## 4 Bluetooth subsystem

### 4.1 2.4 GHz Bluetooth Tx/Rx

- Bluetooth 5.2
- Bluetooth Class 2
- Bluetooth Class 1
- Single-ended, shared Tx/Rx path for Bluetooth (QFN package option)
- Simultaneous Wi-Fi and Bluetooth receive in single-antenna mode (eWLP package option)
- PCM interface for voice applications
- Baseband and radio BDR and EDR packet types—1 Mbit/s (GFSK), 2 Mbit/s ( $\pi/4$ -DQPSK), and 3 Mbit/s (8DPSK)
- Fully functional Bluetooth baseband—AFH, forward error correction, header error control, access code correlation, CRC, encryption bit stream generation, and whitening
- Adaptive Frequency Hopping (AFH) using Packet Error Rate (PER)
- Interlaced scan for faster connection setup
- Simultaneous active ACL connection support
- Automatic ACL packet type selection
- Full central and peripheral piconet support
- Scatternet support
- Standard SDIO and UART HCI transport layer
- HCI layer to integrate with profile stack
- SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement
- All standard SCO/eSCO voice coding
- All standard pairing, authentication, link key, and encryption operations
- Standard Bluetooth power-saving mechanisms (sniff modes, and sniff subrating)
- Enhanced Power Control (EPC)
- Channel Quality Driven Data Rate (CQDDR)
- Wideband Speech (WBS) support (1 WBS link)
- Encryption (AES) support<sup>1</sup>

<sup>1</sup> Refer to 88W8987 errata sheet (ES\_88W8987)

## 4.2 Bluetooth Low Energy (LE)

- Broadcaster, Observer, Central, and Peripheral roles
- Supports link layer topology to be central and peripheral (connects up to 16 links)
- Wi-Fi/Bluetooth coexistence protocol support
- Shared RF with BDR/EDR
- Encryption (AES) support<sup>2</sup>
- Intelligent Adaptive Frequency Hopping (AFH)
- Bluetooth LE Privacy 1.2
- Bluetooth LE Secure Connection<sup>2</sup>
- Bluetooth LE Data Length Extension
- Bluetooth LE Advertising Extension
- 2 Mbit/s Bluetooth LE

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<sup>2</sup> Refer to 88W8987 errata sheet (ES\_88W8987)

### 4.3 Bluetooth host interfaces

- SDIO 3.0
- High-speed UART

### 4.4 Coexistence

- Internal coexistence arbitration for Wi-Fi/Bluetooth

### 4.5 PCM interface

- Central or peripheral mode
- PCM bit width size of 8 bits or 16 bits
- Up to 4 slots with configurable bit width and start positions
- PCM short frame and long frame<sup>3</sup> synchronization
- 3-state PCM interface capability

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<sup>3</sup> In PCM Central mode, PCM long frame synchronization is 1 clock wide. In PCM peripheral mode, PCM central long frame synchronization pattern is supported.

5 Pin information

5.1 Signal diagrams

5.1.1 Signal diagram for QFN package option

Figure 6 shows the signals for the QFN package of the device.

**Note:** Signals may be muxed. See [Section 5.5 "Pin description"](#).

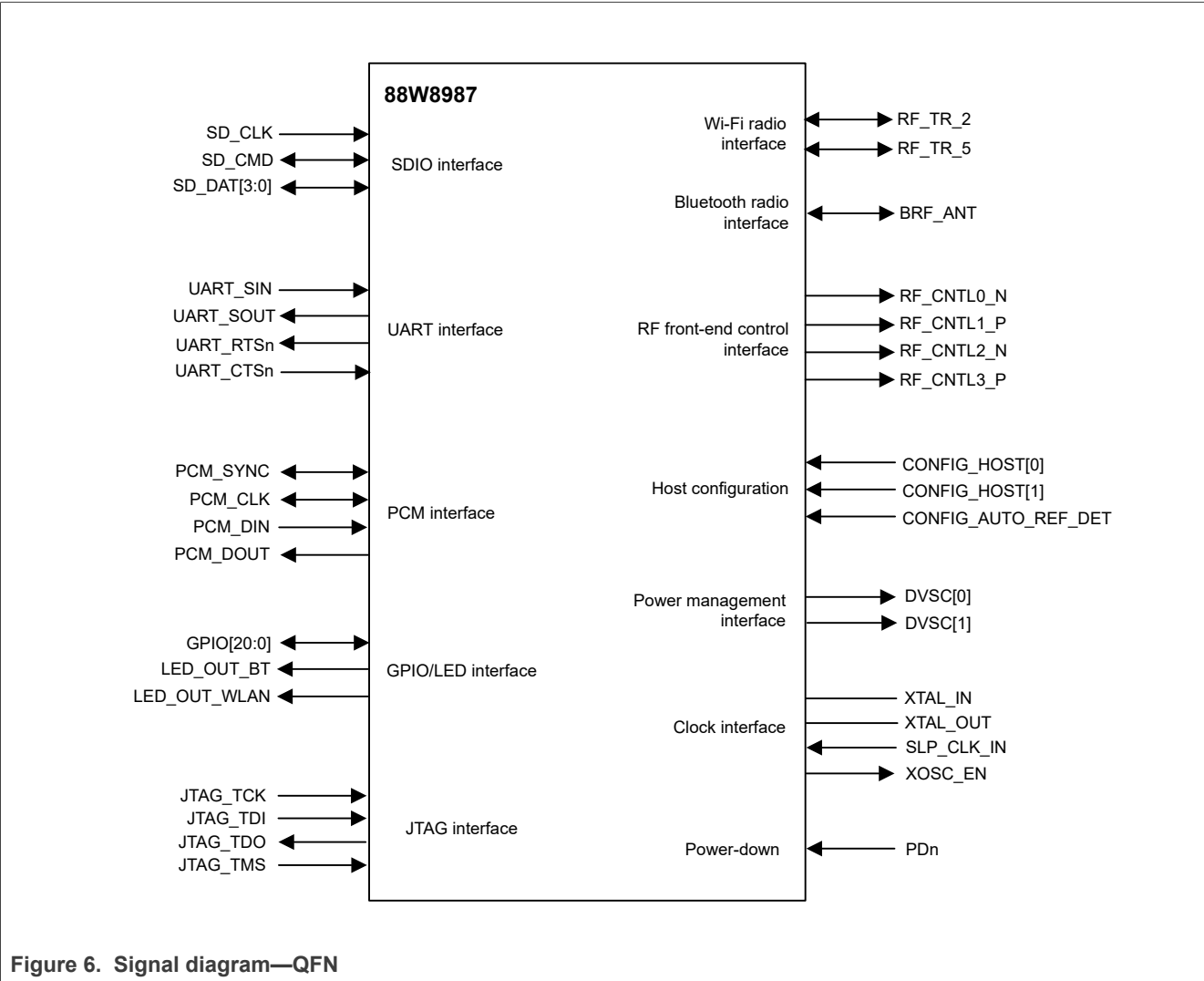
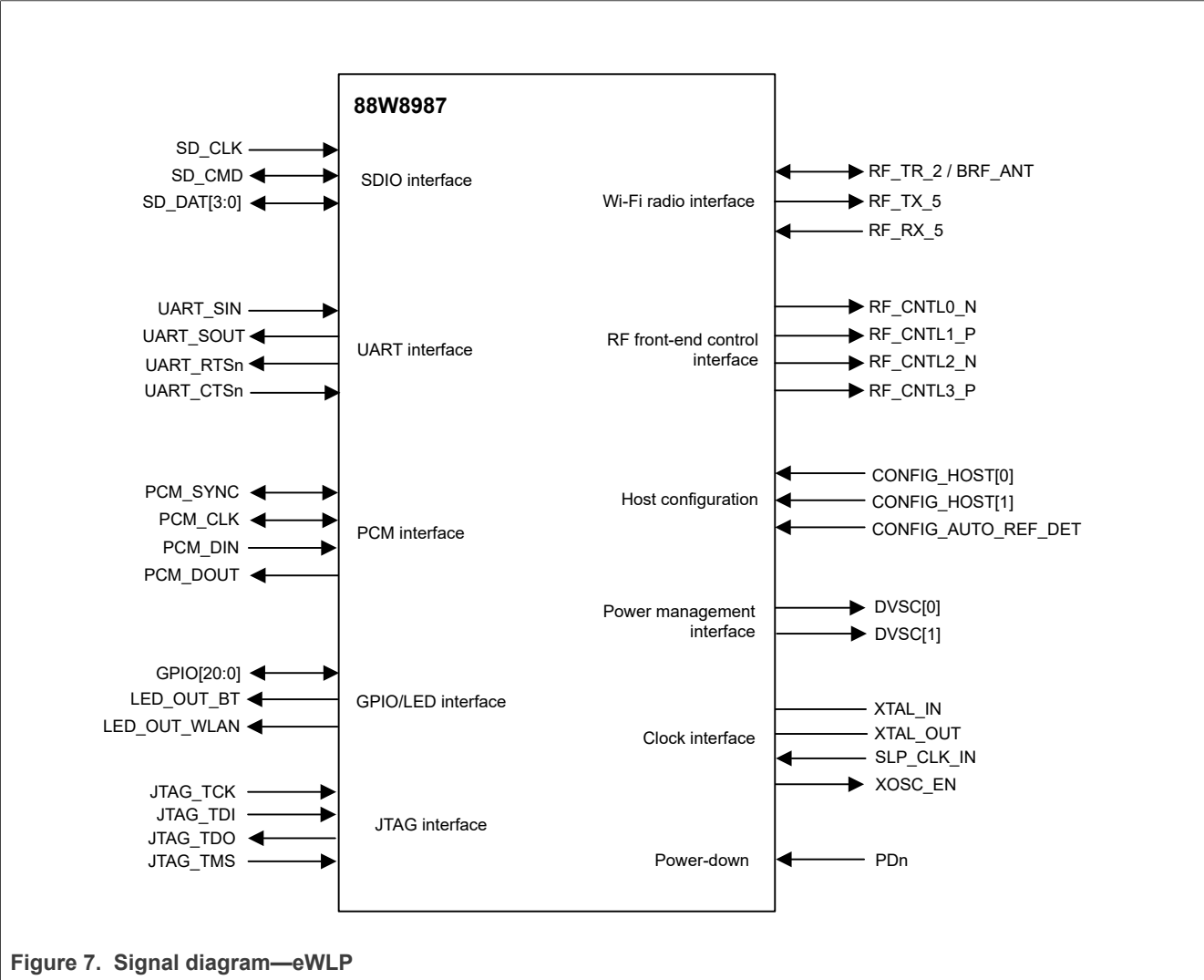


Figure 6. Signal diagram—QFN

5.1.2 Signal diagram for eWLP package option

Figure 7 shows the signals for eWLP package option.

**Note:** Signals may be muxed. See Section 5.5 "Pin description".

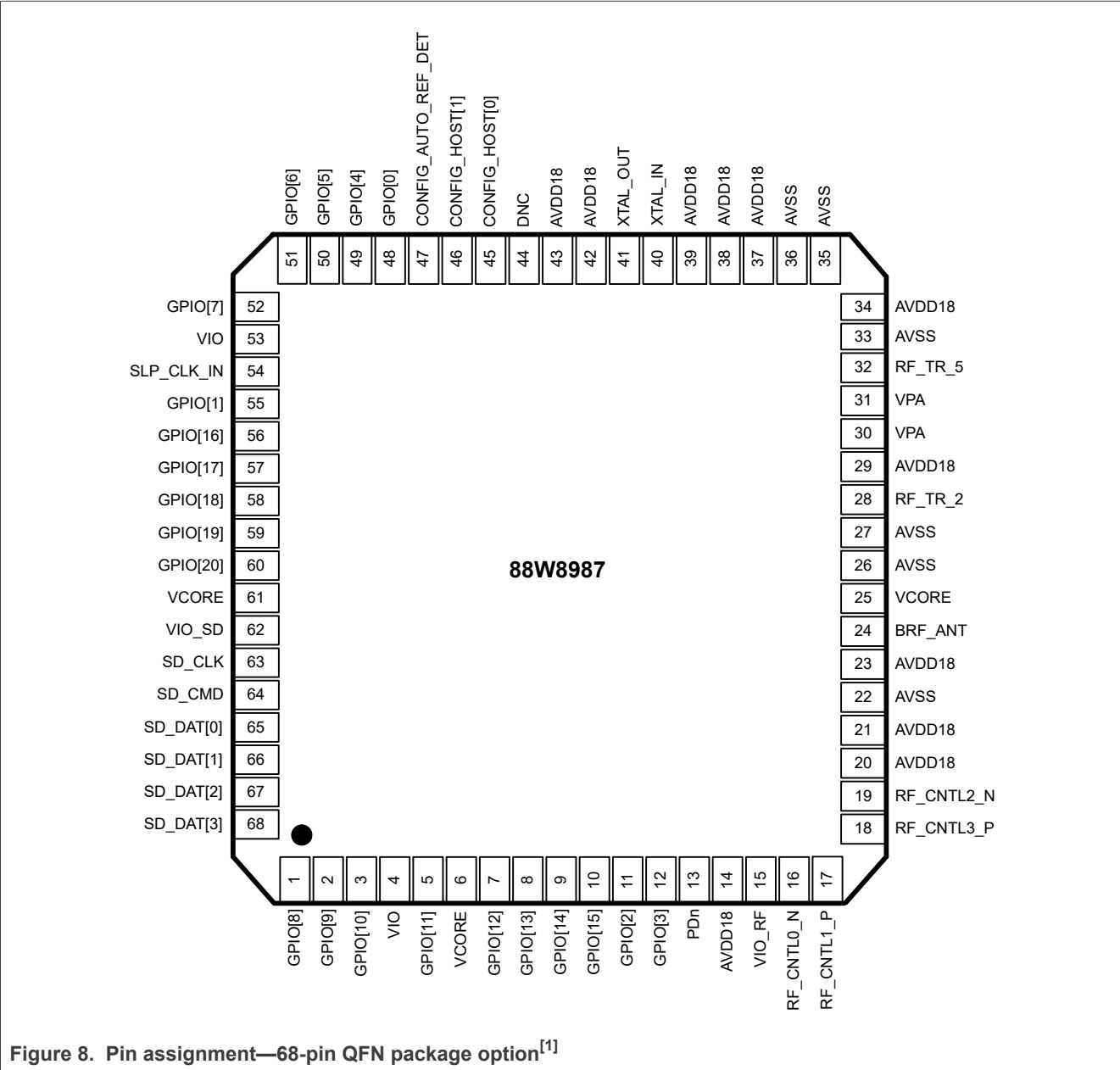


## 5.2 Pin types

Table 2. Pin types

| Pin type | Description          |
|----------|----------------------|
| I/O      | Digital input/output |
| I        | Digital input        |
| O        | Digital output       |
| A, I     | Analog input         |
| A, O     | Analog output        |
| A, I/O   | Analog input/output  |
| NC       | No connect           |
| DNC      | Do not connect       |
| Power    | Power                |
| Ground   | Ground               |

5.3 Pin assignment—68-pin QFN



[1] EPAD on pin 69.

### 5.3.1 Pin list by number

The following table shows the pin list sorted by pin number.

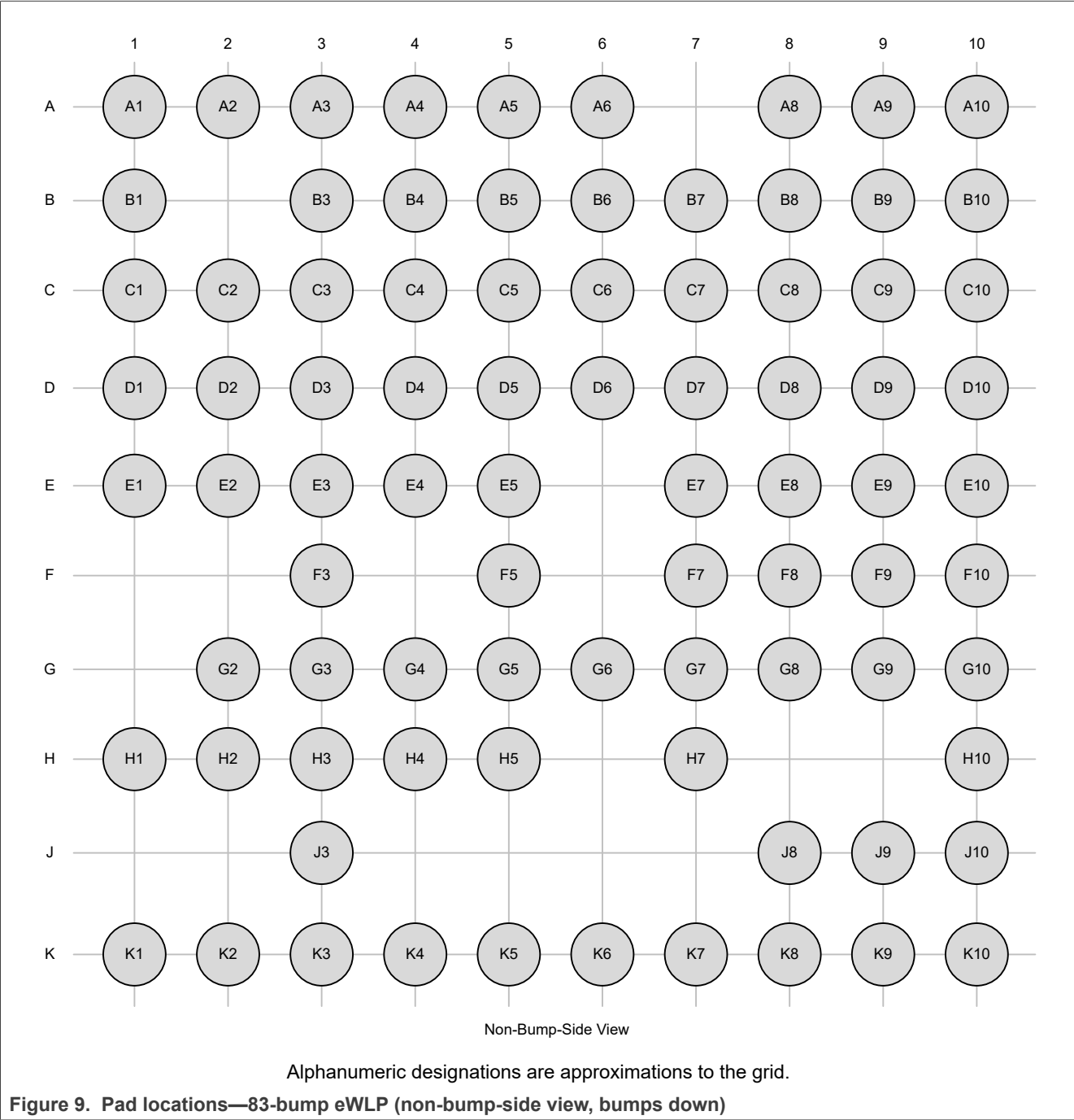
Table 3. Pin list by number

| Pin number | Pin name   | Power  | Type   |
|------------|------------|--------|--------|
| 1          | GPIO[8]    | VIO    | I/O    |
| 2          | GPIO[9]    | VIO    | I/O    |
| 3          | GPIO[10]   | VIO    | I/O    |
| 4          | VIO        | --     | Power  |
| 5          | GPIO[11]   | VIO    | I/O    |
| 6          | VCORE      | --     | Power  |
| 7          | GPIO[12]   | VIO    | I/O    |
| 8          | GPIO[13]   | VIO    | I/O    |
| 9          | GPIO[14]   | VIO    | I/O    |
| 10         | GPIO[15]   | VIO    | I/O    |
| 11         | GPIO[2]    | VIO    | I/O    |
| 12         | GPIO[3]    | VIO    | I/O    |
| 13         | PDn        | AVDD18 | I      |
| 14         | AVDD18     | --     | Power  |
| 15         | VIO_RF     | --     | Power  |
| 16         | RF_CNTL0_N | VIO_RF | O      |
| 17         | RF_CNTL1_P | VIO_RF | O      |
| 18         | RF_CTLN3_P | VIO_RF | O      |
| 19         | RF_CTLN2_N | VIO_RF | O      |
| 20         | AVDD18     | --     | Power  |
| 21         | AVDD18     | --     | Power  |
| 22         | AVSS       | --     | Ground |
| 23         | AVDD18     | --     | Power  |
| 24         | BRF_ANT    | AVDD18 | A, I/O |
| 25         | VCORE      | --     | Power  |
| 26         | AVSS       | --     | Ground |
| 27         | AVSS       | --     | Ground |
| 28         | RF_TR_2    | AVDD18 | A, I/O |
| 29         | AVDD18     | --     | Power  |
| 30         | VPA        | --     | Power  |
| 31         | VPA        | --     | Power  |
| 32         | RF_TR_5    | AVDD18 | A, I/O |
| 33         | AVSS       | --     | Ground |
| 34         | AVDD18     | --     | Power  |

Table 3. Pin list by number...continued

| Pin number | Pin name            | Power  | Type   |
|------------|---------------------|--------|--------|
| 35         | AVSS                | --     | Ground |
| 36         | AVSS                | --     | Ground |
| 37         | AVDD18              | --     | Power  |
| 38         | AVDD18              | --     | Power  |
| 39         | AVDD18              | --     | Power  |
| 40         | XTAL_IN             | AVDD18 | I      |
| 41         | XTAL_OUT            | AVDD18 | O      |
| 42         | AVDD18              | --     | Power  |
| 43         | AVDD18              | --     | Power  |
| 44         | DNC                 | --     | --     |
| 45         | CONFIG_HOST[0]      | AVDD18 | I      |
| 46         | CONFIG_HOST[1]      | AVDD18 | I      |
| 47         | CONFIG_AUTO_REF_DET | AVDD18 | I      |
| 48         | GPIO[0]             | VIO    | I/O    |
| 49         | GPIO[4]             | VIO    | I/O    |
| 50         | GPIO[5]             | VIO    | I/O    |
| 51         | GPIO[6]             | VIO    | I/O    |
| 52         | GPIO[7]             | VIO    | I/O    |
| 53         | VIO                 | --     | Power  |
| 54         | SLP_CLK_IN          | VIO    | I      |
| 55         | GPIO[1]             | VIO    | I/O    |
| 56         | GPIO[16]            | VIO    | I/O    |
| 57         | GPIO[17]            | VIO    | I/O    |
| 58         | GPIO[18]            | VIO    | I/O    |
| 59         | GPIO[19]            | VIO    | I/O    |
| 60         | GPIO[20]            | VIO    | I/O    |
| 61         | VCORE               | --     | Power  |
| 62         | VIO_SD              | --     | Power  |
| 63         | SD_CLK              | VIO_SD | I      |
| 64         | SD_CMD              | VIO_SD | I/O    |
| 65         | SD_DAT[0]           | VIO_SD | I/O    |
| 66         | SD_DAT[1]           | VIO_SD | I/O    |
| 67         | SD_DAT[2]           | VIO_SD | I/O    |
| 68         | SD_DAT[3]           | VIO_SD | I/O    |

5.4 Pad locations—83-bump eWLP



[Table 4](#) indicates the pad locations in 83-bump eWLP package.

**Note:** Alphanumeric designations are approximations to the grid shown in [Figure 9](#)

Table 4. Pad locations—83-bump eWLP

| Signal name       | Alpha-numeric designation | Pad location relative to die center (non-bump-side view) |        |
|-------------------|---------------------------|----------------------------------------------------------|--------|
|                   |                           | X                                                        | Y      |
| NC                | A1                        | -1800.0                                                  | 1800.0 |
| GPIO[18]          | A2                        | -1400.0                                                  | 1800.0 |
| VSS               | A3                        | -1000.0                                                  | 1800.0 |
| GPIO[19]          | A4                        | -600.0                                                   | 1800.0 |
| VCORE             | A5                        | -200.0                                                   | 1800.0 |
| VIO_SD            | A6                        | 200.0                                                    | 1800.0 |
| VSS               | A8                        | 1000.0                                                   | 1800.0 |
| SD_DAT[3]         | A9                        | 1400.0                                                   | 1800.0 |
| VSS               | A10                       | 1800.0                                                   | 1800.0 |
| VIO               | B1                        | -1800.0                                                  | 1400.0 |
| SLP_CLK_IN        | B3                        | -1000.0                                                  | 1400.0 |
| GPIO[16]          | B4                        | -600.0                                                   | 1400.0 |
| GPIO[17]          | B5                        | -200.0                                                   | 1400.0 |
| GPIO[20]          | B6                        | 200.0                                                    | 1400.0 |
| SD_CLK            | B7                        | 600.0                                                    | 1400.0 |
| SD_DAT[0]         | B8                        | 1000.0                                                   | 1400.0 |
| SD_DAT[1]         | B9                        | 1400.0                                                   | 1400.0 |
| SD_DAT[2]         | B10                       | 1800.0                                                   | 1400.0 |
| AVDD18            | C1                        | -1800.0                                                  | 1000.0 |
| AVSS              | C2                        | -1400.0                                                  | 1000.0 |
| GPIO[0] / XOSC_EN | C3                        | -1000.0                                                  | 1000.0 |
| GPIO[6]           | C4                        | -600.0                                                   | 1000.0 |
| GPIO[7]           | C5                        | -200.0                                                   | 1000.0 |
| GPIO[1]           | C6                        | 200.0                                                    | 1000.0 |
| SD_CMD            | C7                        | 600.0                                                    | 1000.0 |
| GPIO[10]          | C8                        | 1000.0                                                   | 1000.0 |
| GPIO[8]           | C9                        | 1400.0                                                   | 1000.0 |
| VIO               | C10                       | 1800.0                                                   | 1000.0 |
| XTAL_IN           | D1                        | -1800.0                                                  | 600.0  |
| XTAL_OUT          | D2                        | -1400.0                                                  | 600.0  |
| DNC               | D3                        | -1000.0                                                  | 600.0  |
| CONFIG_HOST[0]    | D4                        | -600.0                                                   | 600.0  |
| GPIO[4]           | D5                        | -200.0                                                   | 600.0  |
| GPIO[5]           | D6                        | 200.0                                                    | 600.0  |

Table 4. Pad locations—83-bump eWLP...continued

| Signal name         | Alpha-numeric designation | Pad location relative to die center (non-bump-side view) |         |
|---------------------|---------------------------|----------------------------------------------------------|---------|
|                     |                           | X                                                        | Y       |
| GPIO[12]            | D7                        | 600.0                                                    | 600.0   |
| GPIO[9]             | D8                        | 1000.0                                                   | 600.0   |
| GPIO[11]            | D9                        | 1400.0                                                   | 600.0   |
| VCORE               | D10                       | 1800.0                                                   | 600.0   |
| AVDD18              | E1                        | -1800.0                                                  | 200.0   |
| AVSS                | E2                        | -1400.0                                                  | 200.0   |
| AVDD18              | E3                        | -1000.0                                                  | 200.0   |
| AVSS                | E4                        | -600.0                                                   | 200.0   |
| CONFIG_AUTO_REF_DET | E5                        | -200.0                                                   | 200.0   |
| GPIO[13]            | E7                        | 600.0                                                    | 200.0   |
| GPIO[3]             | E8                        | 1000.0                                                   | 200.0   |
| GPIO[15]            | E9                        | 1400.0                                                   | 200.0   |
| GPIO[14]            | E10                       | 1800.0                                                   | 200.0   |
| AVSS                | F3                        | -1000.0                                                  | -200.0  |
| CONFIG_HOST[1]      | F5                        | -200.0                                                   | -200.0  |
| GPIO[2]             | F7                        | 600.0                                                    | -200.0  |
| PDn                 | F8                        | 1000.0                                                   | -200.0  |
| AVDD18              | F9                        | 1400.0                                                   | -200.0  |
| VSS                 | F10                       | 1800.0                                                   | -200.0  |
| AVDD18              | G2                        | -1400.0                                                  | -600.0  |
| AVSS                | G3                        | -1000.0                                                  | -600.0  |
| VCORE               | G4                        | -600.0                                                   | -600.0  |
| AVSS                | G5                        | -200.0                                                   | -600.0  |
| RF_CNTL0_N          | G6                        | 200.0                                                    | -600.0  |
| RF_CNTL1_P          | G7                        | 600.0                                                    | -600.0  |
| RF_CNTL3_P          | G8                        | 1000.0                                                   | -600.0  |
| RF_CNTL2_N          | G9                        | 1400.0                                                   | -600.0  |
| VIO_RF              | G10                       | 1800.0                                                   | -600.0  |
| AVSS                | H1                        | -1800.0                                                  | -1000.0 |
| AVSS                | H2                        | -1400.0                                                  | -1000.0 |
| AVSS                | H3                        | -1000.0                                                  | -1000.0 |
| AVSS                | H4                        | -600.0                                                   | -1000.0 |
| AVSS                | H5                        | -200.0                                                   | -1000.0 |
| AVSS                | H7                        | 600.0                                                    | -1000.0 |

Table 4. Pad locations—83-bump eWLP...continued

| Signal name       | Alpha-numeric designation | Pad location relative to die center (non-bump-side view) |         |
|-------------------|---------------------------|----------------------------------------------------------|---------|
|                   |                           | X                                                        | Y       |
| AVSS              | H10                       | 1800.0                                                   | -1000.0 |
| VPA               | J3                        | -1000.0                                                  | -1400.0 |
| AVSS              | J8                        | 1000.0                                                   | -1400.0 |
| AVSS              | J9                        | 1400.0                                                   | -1400.0 |
| AVSS              | J10                       | 1800.0                                                   | -1400.0 |
| NC                | K1                        | -1800.0                                                  | -1800.0 |
| RF_RX_5           | K2                        | -1400.0                                                  | -1800.0 |
| RF_TX_5           | K3                        | -1000.0                                                  | -1800.0 |
| RF_TR_2 / BRF_ANT | K4                        | -600.0                                                   | -1800.0 |
| AVDD18            | K5                        | -200.0                                                   | -1800.0 |
| AVSS              | K6                        | 200.0                                                    | -1800.0 |
| AVDD18            | K7                        | 600.0                                                    | -1800.0 |
| AVDD18            | K8                        | 1000.0                                                   | -1800.0 |
| AVDD18            | K9                        | 1400.0                                                   | -1800.0 |
| NC                | K10                       | 1800.0                                                   | -1800.0 |

## 5.5 Pin description

### 5.5.1 Pin states

The pin states information provided in the tables includes:

- **No Pad Power State** indicates the state when there is no power
- **PwrDwn State** denotes the power-down state in the default configuration. Many pads have programmable power-down values which can be set by firmware.
- **Reset State** is the state after the power-on-reset state and before the hardware state (HW State)
- **HW State** (hardware state) is the state after the boot code finishes and before the firmware download begins (firmware may change the pin state). HW State may differ based on the pin muxing/configuration setting. For example, for UART\_RTSn and UART\_SOUT, the boot code enables the UART interface when the device is in PCIe-UARTSDIO-UART mode, making the HW states output high and output low, respectively.
- **PwrDwn Prog** indicates if the power-down state can be programmed
- **Internal PU/PD** columns indicates the following:
  - Type of PU/PD (weak vs nominal)
  - The polarity (PU vs. PD)

The internal pull-up or pull-down applies when the pin is in input mode
- **PU** denotes whether the pull-up can be programmed or not
- **PD** denotes whether the pull-down can be programmed or not
- Pull-up and pull-down are only effective when the pad is in input mode
- At the end of the firmware download, the pads (for example GPIO and RF control) are programmed in the functional mode corresponding to the functionality of the pins

### 5.5.2 General purpose I/O (GPIO)

Table 5. General purpose I/O (GPIO)<sup>[1]</sup> (MFP)

Pins may be Multi-Functional Pins (MFP).

| Pin Name                                                                                                                      | Supply | No Pad Power State <sup>[2]</sup> | Reset State | HW State                   | PwrDwn State | PwrDwn Prog | Internal PU/PD | PU  | PD  |
|-------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------|-------------|----------------------------|--------------|-------------|----------------|-----|-----|
| GPIO[20]                                                                                                                      | VIO    | tristate                          | output      | output high <sup>[3]</sup> | tristate     | yes         | weak PU        | yes | yes |
| <b>GPIO Mode:</b> GPIO[20] (input/output).<br>This pin can be used for Bluetooth to host wake-up (out-of-band wake-up signal) |        |                                   |             |                            |              |             |                |     |     |
| GPIO[19]                                                                                                                      | VIO    | tristate                          | output      | output high                | tristate     | yes         | weak PU        | yes | yes |
| <b>GPIO Mode:</b> GPIO[19] (input/output)<br><b>Power Management Mode:</b> DVSC[1] digital voltage scaling control (output)   |        |                                   |             |                            |              |             |                |     |     |
| GPIO[18]                                                                                                                      | VIO    | tristate                          | output      | output high                | tristate     | yes         | weak PU        | yes | yes |
| <b>GPIO Mode:</b> GPIO[18] (input/output)<br><b>Power Management Mode:</b> DVSC[0] digital voltage scaling control (output)   |        |                                   |             |                            |              |             |                |     |     |
| GPIO[17]                                                                                                                      | VIO    | tristate                          | input       | input                      | tristate     | yes         | weak PU        | yes | yes |

Table 5. General purpose I/O (GPIO)<sup>[1]</sup> (MFP)...continued

Pins may be Multi-Functional Pins (MFP).

| Pin Name                                                                                                                                                                                                            | Supply | No Pad Power State <sup>[2]</sup> | Reset State | HW State                                      | PwrDwn State | PwrDwn Prog | Internal PU/ PD | PU  | PD  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------|-------------|-----------------------------------------------|--------------|-------------|-----------------|-----|-----|
| <b>GPIO Mode:</b> GPIO[17] (input/output)<br><b>JTAG Mode:</b> JTAG_TDO, JTAG test data (output)<br>This pin is used as a configuration pin: CON[9] (input). See <a href="#">Section 5.6 "Configuration pins"</a> . |        |                                   |             |                                               |              |             |                 |     |     |
| GPIO[16]                                                                                                                                                                                                            | VIO    | tristate                          | input       | input                                         | tristate     | yes         | nominal PU      | yes | yes |
| <b>GPIO Mode:</b> GPIO[16] (input/output)<br><b>JTAG Mode:</b> JTAG_TDI, JTAG test data (input)                                                                                                                     |        |                                   |             |                                               |              |             |                 |     |     |
| GPIO[15]                                                                                                                                                                                                            | VIO    | tristate                          | input       | input                                         | output high  | yes         | nominal PU      | yes | yes |
| <b>GPIO Mode:</b> GPIO[15] (input/output).<br>This pin can also be used as Bluetooth independent reset.<br><b>JTAG Mode:</b> JTAG_TMS, JTAG controller select (input)                                               |        |                                   |             |                                               |              |             |                 |     |     |
| GPIO[14]                                                                                                                                                                                                            | VIO    | tristate                          | input       | input                                         | tristate     | yes         | nominal PU      | yes | yes |
| <b>GPIO Mode:</b> GPIO[14] (input/output)<br>This pin can also be used as Wi-Fi independent reset.<br><b>JTAG Mode:</b> JTAG_TCK, JTAG test clock (input)                                                           |        |                                   |             |                                               |              |             |                 |     |     |
| GPIO[13]                                                                                                                                                                                                            | VIO    | tristate                          | input       | input <sup>[4]</sup><br>output <sup>[5]</sup> | output high  | yes         | nominal PU      | yes | yes |
| <b>GPIO Mode:</b> GPIO[13] (input/output)<br>This pin can also be used for host to 88W8987 Wi-Fi wake-up (out-of-band wake-up signal).                                                                              |        |                                   |             |                                               |              |             |                 |     |     |
| GPIO[12]                                                                                                                                                                                                            | VIO    | tristate                          | input       | input                                         | tristate     | yes         | nominal PU      | yes | yes |
| <b>GPIO Mode:</b> GPIO[12] (input/output)<br>This pin can also be used for host to 88W8987 Bluetooth wake-up (out-of-band wake-up signal)                                                                           |        |                                   |             |                                               |              |             |                 |     |     |
| GPIO[11]                                                                                                                                                                                                            | VIO    | tristate                          | input       | input <sup>[4]</sup><br>output <sup>[5]</sup> | output high  | yes         | weak PU         | yes | yes |
| <b>GPIO Mode:</b> GPIO[11] (input/output)<br><b>UART Mode:</b> UART_RTSn (output) (active low)<br>This pin is used as a configuration pin: CON[8] (input). See <a href="#">Section 5.6 "Configuration pins"</a> .   |        |                                   |             |                                               |              |             |                 |     |     |
| GPIO[10]                                                                                                                                                                                                            | VIO    | tristate                          | input       | input                                         | tristate     | yes         | nominal PU      | yes | yes |
| <b>GPIO Mode:</b> GPIO[10] (input/output)<br><b>UART Mode:</b> UART_CTSn (input) (active low)                                                                                                                       |        |                                   |             |                                               |              |             |                 |     |     |
| GPIO[9]                                                                                                                                                                                                             | VIO    | tristate                          | input       | input                                         | tristate     | yes         | nominal PU      | yes | yes |
| <b>GPIO Mode:</b> GPIO[9] (input/output)<br><b>UART Mode:</b> UART_SIN (input)                                                                                                                                      |        |                                   |             |                                               |              |             |                 |     |     |
| GPIO[8]                                                                                                                                                                                                             | VIO    | tristate                          | input       | input <sup>[4]</sup><br>output <sup>[5]</sup> | output low   | yes         | weak PU         | yes | yes |
| <b>GPIO Mode:</b> GPIO[8] (input/output)<br><b>UART Mode:</b> UART_SOUT (output)<br>This pin is used as a configuration pin: CONFIG_XOSC_SEL (input). See <a href="#">Section 5.6 "Configuration pins"</a> .        |        |                                   |             |                                               |              |             |                 |     |     |

**Table 5. General purpose I/O (GPIO)<sup>[1]</sup> (MFP)...***continued**Pins may be Multi-Functional Pins (MFP).*

| Pin Name                                                                                                                                                                                          | Supply | No Pad Power State <sup>[2]</sup> | Reset State | HW State                   | PwrDwn State | PwrDwn Prog | Internal PU/ PD | PU  | PD  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------|-------------|----------------------------|--------------|-------------|-----------------|-----|-----|
| GPIO[7]                                                                                                                                                                                           | VIO    | tristate                          | input       | input                      | tristate     | yes         | nominal PU      | yes | yes |
| <b>GPIO Mode:</b> GPIO[7] (input/output)<br><b>PCM Mode:</b> PCM_SYNC (input/output) <ul style="list-style-type: none"> <li>• Output if central</li> <li>• Input if peripheral</li> </ul>         |        |                                   |             |                            |              |             |                 |     |     |
| GPIO[6]                                                                                                                                                                                           | VIO    | tristate                          | input       | input                      | tristate     | yes         | nominal PU      | yes | yes |
| <b>GPIO Mode:</b> GPIO[6] (input/output)<br><b>PCM Mode:</b> PCM_CLK (input/output) <ul style="list-style-type: none"> <li>• Output if central</li> <li>• Input if peripheral</li> </ul>          |        |                                   |             |                            |              |             |                 |     |     |
| GPIO[5]                                                                                                                                                                                           | VIO    | tristate                          | input       | input                      | tristate     | yes         | weak PU         | yes | yes |
| <b>GPIO Mode:</b> GPIO[5] (input/output)<br><b>PCM Mode:</b> PCM_DOUT (output)<br>This pin is used as a configuration pin: CON[7] (input). See <a href="#">Section 5.6 "Configuration pins"</a> . |        |                                   |             |                            |              |             |                 |     |     |
| GPIO[4]                                                                                                                                                                                           | VIO    | tristate                          | input       | input                      | tristate     | yes         | nominal PU      | yes | yes |
| <b>GPIO Mode:</b> GPIO[4] (input/output)<br><b>PCM Mode:</b> PCM_DIN (input)                                                                                                                      |        |                                   |             |                            |              |             |                 |     |     |
| GPIO[3]                                                                                                                                                                                           | VIO    | tristate                          | output      | output high <sup>[3]</sup> | tristate     | yes         | weak PU         | yes | yes |
| <b>GPIO Mode:</b> GPIO[3] (input/output)<br><b>LED Mode:</b> LED_OUT_BT (output)                                                                                                                  |        |                                   |             |                            |              |             |                 |     |     |
| GPIO[2]                                                                                                                                                                                           | VIO    | tristate                          | output      | output high <sup>[3]</sup> | tristate     | yes         | weak PU         | yes | yes |
| <b>GPIO Mode:</b> GPIO[2] (input/output)<br><b>LED Mode:</b> LED_OUT_WLAN (output)                                                                                                                |        |                                   |             |                            |              |             |                 |     |     |
| GPIO[1]                                                                                                                                                                                           | VIO    | tristate                          | input       | input                      | tristate     | yes         | weak PU         | yes | yes |
| <b>GPIO Mode:</b> GPIO[1] (input/output).<br>This pin can also be used for 88W8987 Wi-Fi to host wake-up (out-of-band wake-up signal).                                                            |        |                                   |             |                            |              |             |                 |     |     |
| GPIO[0]                                                                                                                                                                                           | VIO    | tristate                          | output      | output high                | output low   | yes         | nominal PU      | yes | no  |
| <b>GPIO Mode:</b> GPIO[0] (input/output)<br><b>Oscillator Enable Mode:</b> XOSC_EN (output) (active high). See <a href="#">Section 5.5.9 "Clock interface"</a> .                                  |        |                                   |             |                            |              |             |                 |     |     |

[1] Not all GPIO pins can be used for Host-to-SoC wake-up signals.

[2] Maximum input voltage is 0.4V when VIO has no power (or in uncertain situations).

[3] The signal may toggle while boot code is executing.

[4] When the device is in SDIO-SDIO mode.

[5] When the device is in SDIO-UART mode.

### 5.5.3 Wi-Fi/Bluetooth radio interface

Table 6. Wi-Fi/Bluetooth radio interface - QFN package

| Pin Name | Type   | Supply | Description                      |
|----------|--------|--------|----------------------------------|
| RF_TR_2  | A, I/O | AVDD18 | Wi-Fi Transmit/Receive (2.4 GHz) |
| RF_TR_5  | A, I/O | AVDD18 | Wi-Fi Transmit/Receive (5 GHz)   |
| BRF_ANT  | A, I/O | AVDD18 | Bluetooth Transmit/Receive       |

Table 7. Wi-Fi/Bluetooth radio interface - eWLP package option

| Pin Name        | Type   | Supply | Description                                                                                          |
|-----------------|--------|--------|------------------------------------------------------------------------------------------------------|
| RF_TR_2/BRF_ANT | A, I/O | AVDD18 | Wi-Fi Transmit/Receive (2.4 GHz)<br>Bluetooth Transmit/Receive (shared path for Wi-Fi and Bluetooth) |
| RF_RX_5         | A, I   | AVDD18 | Wi-Fi Receive (5 GHz)                                                                                |
| RF_TX_5         | A, O   | AVDD18 | Wi-Fi Transmit (5 GHz)                                                                               |

### 5.5.4 Wi-Fi RF front-end control interface

Table 8. Wi-Fi RF front-end control interface

| Pin Name                                                                                                                                                        | Supply | No Pad Power State <sup>[1]</sup> | Reset State | HW State | PwrDwn State | PwrDwn Prog | Internal PU/PD | PU | PD |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------|-------------|----------|--------------|-------------|----------------|----|----|
| RF_CNTL0_N                                                                                                                                                      | VIO_RF | tristate                          | output      | output   | drive low    | yes         | nominal PU     | no | no |
| RF Control 0—RF Control Output Low (output)                                                                                                                     |        |                                   |             |          |              |             |                |    |    |
| RF_CNTL1_P                                                                                                                                                      | VIO_RF | tristate                          | output      | output   | drive high   | yes         | weak PU        | no | no |
| RF Control 1—RF Control Output High (output)<br>This pin is used as a configuration pin: CON[6] (input). See <a href="#">Section 5.6 "Configuration pins"</a> . |        |                                   |             |          |              |             |                |    |    |
| RF_CNTL2_N                                                                                                                                                      | VIO_RF | tristate                          | output      | output   | drive low    | yes         | weak PU        | no | no |
| RF Control 2—RF Control Output Low (output)                                                                                                                     |        |                                   |             |          |              |             |                |    |    |
| RF_CNTL3_P                                                                                                                                                      | VIO_RF | tristate                          | output      | output   | drive high   | yes         | weak PU        | no | no |
| RF Control 3—RF Control Output High (output)                                                                                                                    |        |                                   |             |          |              |             |                |    |    |

[1] Maximum input voltage is 0.4V when VIO\_RF has no power (or in uncertain situations).

### 5.5.5 SDIO host interface

Table 9. SDIO host interface

| Pin Name                                                                                                         | Supply | No Pad Power State <sup>[1]</sup> | Reset State | HW State | PwrDwn State | PwrDwn Prog | Internal PU/ PD | PU  | PD  |
|------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------|-------------|----------|--------------|-------------|-----------------|-----|-----|
| SD_CLK                                                                                                           | VIO_SD | tristate                          | input       | input    | tristate     | no          | nominal PU      | yes | yes |
| <b>SDIO 4-bit Mode:</b> Clock input<br><b>SDIO 1-bit Mode:</b> Clock input                                       |        |                                   |             |          |              |             |                 |     |     |
| SD_CMD                                                                                                           | VIO_SD | tristate                          | input       | input    | tristate     | no          | nominal PU      | yes | yes |
| <b>SDIO 4-bit Mode:</b> Command/response (input/output)<br><b>SDIO 1-bit Mode:</b> Command line                  |        |                                   |             |          |              |             |                 |     |     |
| SD_DAT[3]                                                                                                        | VIO_SD | tristate                          | input       | input    | tristate     | no          | nominal PU      | yes | yes |
| <b>SDIO 4-bit Mode:</b> Data line Bit[3]<br><b>SDIO 1-bit Mode:</b> Reserved                                     |        |                                   |             |          |              |             |                 |     |     |
| SD_DAT[2]                                                                                                        | VIO_SD | tristate                          | input       | input    | tristate     | no          | nominal PU      | yes | yes |
| <b>SDIO 4-bit Mode:</b> Data line Bit[2] or read wait (optional)<br><b>SDIO 1-bit Mode:</b> Read wait (optional) |        |                                   |             |          |              |             |                 |     |     |
| SD_DAT[1]                                                                                                        | VIO_SD | tristate                          | input       | input    | tristate     | no          | nominal PU      | yes | yes |
| <b>SDIO 4-bit Mode:</b> Data line Bit[1]<br><b>SDIO 1-bit Mode:</b> Interrupt                                    |        |                                   |             |          |              |             |                 |     |     |
| SD_DAT[0]                                                                                                        | VIO_SD | tristate                          | input       | input    | tristate     | no          | nominal PU      | yes | yes |
| <b>SDIO 4-bit Mode:</b> Data line Bit[0]<br><b>SDIO 1-bit Mode:</b> Data line                                    |        |                                   |             |          |              |             |                 |     |     |

[1] Maximum input voltage is 0.4V when VIO\_SD has no power (or in uncertain situations).

### 5.5.6 UART host interface

Table 10. UART host interface (MFP)

Pins may be Multi-Functional Pins (MFP).

| Pin Name  | Type | Supply | Description                                                             |
|-----------|------|--------|-------------------------------------------------------------------------|
| UART_SIN  | I    | VIO    | UART serial input signal - GPIO[9] input/output                         |
| UART_SOUT | O    | VIO    | UART serial output signal - GPIO[8] input/output                        |
| UART_RTSn | O    | VIO    | UART request-to-send output signal . Active low - GPIO[11] input/output |
| UART_CTSn | I    | VIO    | UART clear-to-send input signal - Active low - GPIO[10] input/output    |

### 5.5.7 Audio interface

**Table 11. Audio interface pins (MFP)**

*Pins may be Multi-Functional Pins (MFP).*

| Pin Name | Type | Supply | Description                                                                                                                           |
|----------|------|--------|---------------------------------------------------------------------------------------------------------------------------------------|
| PCM_DIN  | I    | VIO    | Receive PCM input signal. GPIO[4] input/output                                                                                        |
| PCM_DOUT | O    | VIO    | Transmit PCM output signal. GPIO[5] input/output                                                                                      |
| PCM_CLK  | I/O  | VIO    | PCM data clock. GPIO[6] input/output <ul style="list-style-type: none"> <li>Output if central</li> <li>Input if peripheral</li> </ul> |
| PCM_SYNC | I/O  | VIO    | PCM frame sync. GPIO[7] input/output <ul style="list-style-type: none"> <li>Output if central</li> <li>Input if peripheral</li> </ul> |

### 5.5.8 Configuration interface

**Table 12. Configuration interface**

| Pin Name                                                                                                                     | Supply | No Pad Power State | Reset State | HW State | PwrDwn State | PwrDwn Prog | Internal PU/PD | PU  | PD  |
|------------------------------------------------------------------------------------------------------------------------------|--------|--------------------|-------------|----------|--------------|-------------|----------------|-----|-----|
| CONFIG_HOST[0]                                                                                                               | AVDD18 | tristate           | input       | input    | tristate     | no          | weak PU        | yes | yes |
| This pin is used as a configuration pin: CONFIG_HOST[0] (input). See <a href="#">Section 5.6 "Configuration pins"</a> .      |        |                    |             |          |              |             |                |     |     |
| CONFIG_HOST[1]                                                                                                               | AVDD18 | tristate           | input       | input    | tristate     | no          | weak PU        | yes | yes |
| This pin is used as a configuration pin: CONFIG_HOST[1] (input). See <a href="#">Section 5.6 "Configuration pins"</a> .      |        |                    |             |          |              |             |                |     |     |
| CONFIG_AUTO_REF_DET                                                                                                          | AVDD18 | tristate           | input       | input    | tristate     | no          | weak PU        | yes | yes |
| This pin is used as a configuration pin: CONFIG_AUTO_REF_DET (input). See <a href="#">Section 5.6 "Configuration pins"</a> . |        |                    |             |          |              |             |                |     |     |

### 5.5.9 Clock interface

Table 13. Clock interface (MFP)

Pins may be Multi-Functional Pins (MFP).

| Pin Name                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Supply | No Pad Power State <sup>[1]</sup> | Reset State          | HW State | PwrDwn State | PwrDwn Prog | Internal PU/ PD | PU  | PD  |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------------------------------|----------------------|----------|--------------|-------------|-----------------|-----|-----|
| XTAL_IN                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | AVDD18 | --                                | --                   | --       | --           | --          | --              | --  | --  |
| Reference Clock Input<br>Reference clock signal frequency must be 26 MHz or 38.4 MHz from an external crystal or external crystal oscillator.<br>Power consumption in sleep mode is lower with an external crystal compared to an external crystal oscillator when an external sleep clock is not used.<br>See <a href="#">Section 9.9 "Reference clock specifications"</a> .                                                                                            |        |                                   |                      |          |              |             |                 |     |     |
| XTAL_OUT                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | AVDD18 | --                                | --                   | --       | --           | --          | --              | --  | --  |
| Connect this pin to an external crystal when an external crystal is used.<br>When an external crystal oscillator is used, connect this pin to ground with resistance less than 5 kΩ.                                                                                                                                                                                                                                                                                     |        |                                   |                      |          |              |             |                 |     |     |
| SLP_CLK_IN                                                                                                                                                                                                                                                                                                                                                                                                                                                               | VIO    | tristate                          | input <sup>[2]</sup> | input    | tristate     | no          | nominal PU      | yes | yes |
| Sleep Clock Input (optional)<br>Used for lower power operation in sleep mode. <ul style="list-style-type: none"> <li>An external sleep clock of 32.768 kHz can be used for lowest current consumption in sleep mode.</li> <li>An external sleep clock is required if automatic reference clock frequency detection is used. See <a href="#">Section 5.6 "Configuration pins"</a>.</li> <li>If no external sleep clock is used, leave this pin floating (DNC).</li> </ul> |        |                                   |                      |          |              |             |                 |     |     |
| XOSC_EN                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | VIO    | --                                | --                   | --       | --           | --          | --              | --  | --  |
| Oscillator Enable (output) (active high)<br>XOSC_EN signal can be used ONLY when an external sleep clock is used.<br>Used to enable an external oscillator.<br>0 = disable external oscillator<br>1 = enable external oscillator<br>NOTE: Muxed with GPIO[0].                                                                                                                                                                                                            |        |                                   |                      |          |              |             |                 |     |     |

[1] Maximum input voltage is 0.4V when VIO has no power (or in uncertain situations).

[2] Input mode after reset

### 5.5.10 Power down (PDn) pin

Table 14. Power down (PDn) pin

| Pin Name                                                                                                                                                                                                                                                                                             | Supply | No Pad Power State | Reset State | HW State | PwrDwn State | PwrDwn Prog | Internal PU/ PD | PU | PD |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------------------|-------------|----------|--------------|-------------|-----------------|----|----|
| PDn                                                                                                                                                                                                                                                                                                  | AVDD18 | --                 | --          | --       | --           | --          | --              | -- | -- |
| Full Power-down (input) (active low)<br>0 = full power-down mode<br>1 = normal mode <ul style="list-style-type: none"> <li>PDn can accept an input of 1.8V to 4.5V</li> <li>PDn may be driven by the host</li> <li>PDn must be high for normal operation</li> </ul> No internal pull-up on this pin. |        |                    |             |          |              |             |                 |    |    |

### 5.5.11 Power supply and ground

**Table 15. Power supply and ground**

| Pin Name | Type   | Description                                                             |
|----------|--------|-------------------------------------------------------------------------|
| VCORE    | Power  | 1.10V Core Power Supply                                                 |
| VIO      | Power  | 1.8V/3.3V Digital I/O Power Supply                                      |
| VIO_SD   | Power  | 1.8V Digital I/O SDIO Power Supply                                      |
| VIO_RF   | Power  | 1.8V/3.3V Analog I/O RF Power Supply                                    |
| AVDD18   | Power  | 1.8V Analog Power Supply                                                |
| VPA      | Power  | 2.2V Analog Power Supply                                                |
| AVSS     | Ground | Ground                                                                  |
| NC       | NC     | Not Connected                                                           |
| DNC      | DNC    | Do Not Connect<br>Do not connect these pins. Leave these pins floating. |

## 5.6 Configuration pins

[Table 16](#) shows the pins used as configuration inputs to set parameters following a reset. The definition of these pins changes immediately after reset to their usual function.

To set a configuration bit to 0, attach a 50 kΩ–100 kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1.

See [Section 9.11 "Configuration pin specifications"](#) for the internal pull-up values of the configuration pins.

**Table 16. Configuration pins**

| Configuration Bits  | Pin Name            | Configuration Function                                                                                                                                                                                                                 |
|---------------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CON[9]              | GPIO[17]            | Reserved                                                                                                                                                                                                                               |
| CON[8]              | GPIO[11]            | Set to 1.                                                                                                                                                                                                                              |
| CON[7]              | GPIO[5]             |                                                                                                                                                                                                                                        |
| CON[6]              | RF_CNTL1_P          | Reserved<br>Set to 1.                                                                                                                                                                                                                  |
| CONFIG_XOSC_SEL     | GPIO[8]/UART_SOUT   | Reference clock frequency select<br>Valid when CONFIG_AUTO_REF_DET = 0<br>0 = 38.4 MHz<br>1 = 26 MHz (default)                                                                                                                         |
| CONFIG_AUTO_REF_DET | CONFIG_AUTO_REF_DET | Reference clock frequency detection select<br>0 = reference clock frequency detection by CONFIG_XOSC_SEL<br>1 = reference clock frequency detection using external sleep clock (default)(valid only when external sleep clock is used) |
| CON[1]              | CONFIG_HOST[1]      | Host configuration options                                                                                                                                                                                                             |
| CON[0]              | CONFIG_HOST[0]      | No hardware impact. Software reads and boots accordingly. See <a href="#">Table 17</a> .                                                                                                                                               |

**Table 17. Host configuration options**

| Strap Value   | Wi-Fi | Bluetooth/<br>Bluetooth LE | Number of SDIO Functions |
|---------------|-------|----------------------------|--------------------------|
| 00 (reserved) | --    | --                         | --                       |
| 01 (reserved) | --    | --                         | --                       |
| 10            | SDIO  | UART                       | 1 (Wi-Fi)                |
| 11            | SDIO  | SDIO                       | 2 (Wi-Fi, Bluetooth)     |

## 6 Power information

[Section 5.5.11 "Power supply and ground"](#) shows the required voltage levels for each rail and for PDn input signal.

### 6.1 Power-up sequence

- VIO/VIO\_RF must be good (90%) before or at the same time all other power supplies start ramping up.
- VIO/VIO\_RF must be good (90%) before or at the same time PDn starts ramping up.
- VPA must be good (90%) before or at the same time AVDD18 starts ramping up.
- It is recommended to start ramping up AVDD18  $\leq 1$  ms after VPA ramps up.
- AVDD18 must be good (90%) before or at the same time VCORE starts ramping up.
- Ramp-up time of VIO/VIO\_RF must be  $< 100$  ms.
- Ramp-up time of VPA must be  $< 100$  ms.
- Ramp-up time of AVDD18 must be  $< 100$  ms.
- Ramp-up time of VCORE must be  $< 5$  ms.
- All supplies must be monotonic.
- If using an external crystal oscillator, the reference clock must be stable before PDn ramps up.

[Figure 10](#) shows the power-up sequence.

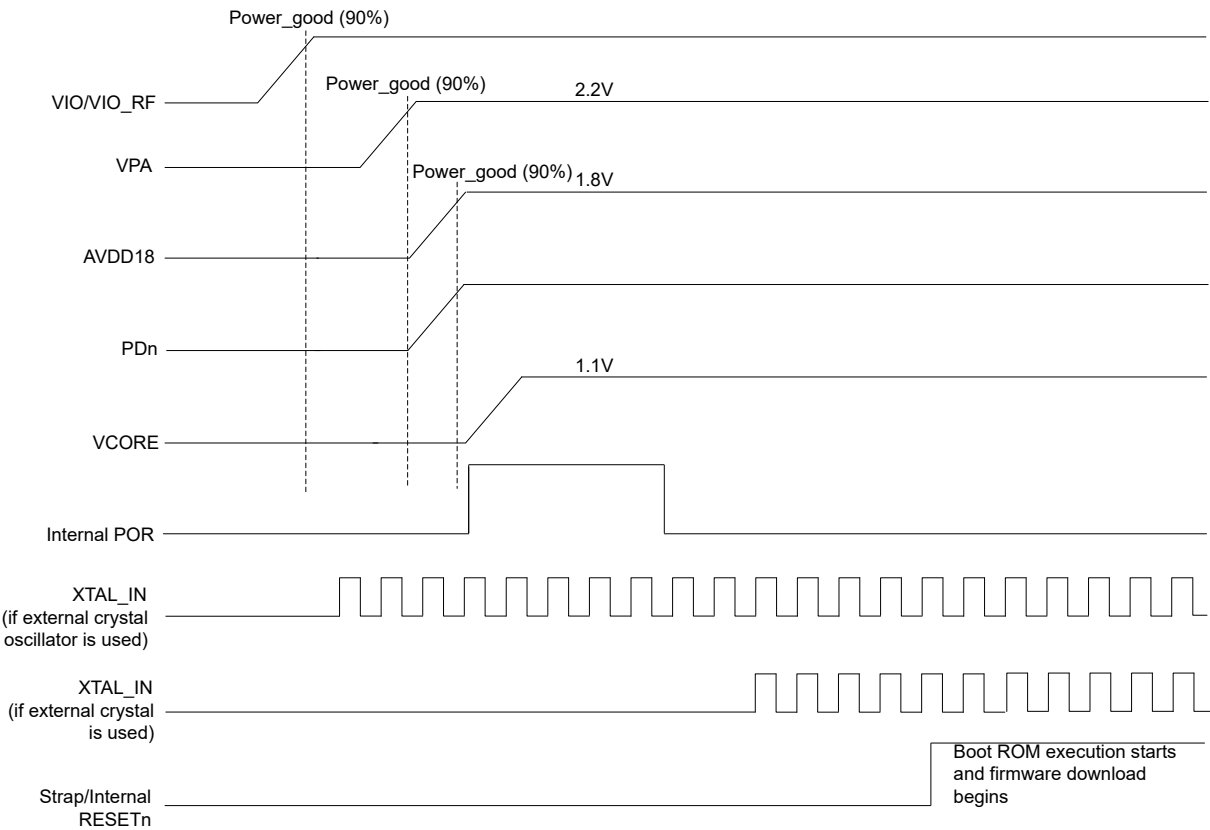


Figure 10. Power-up sequence

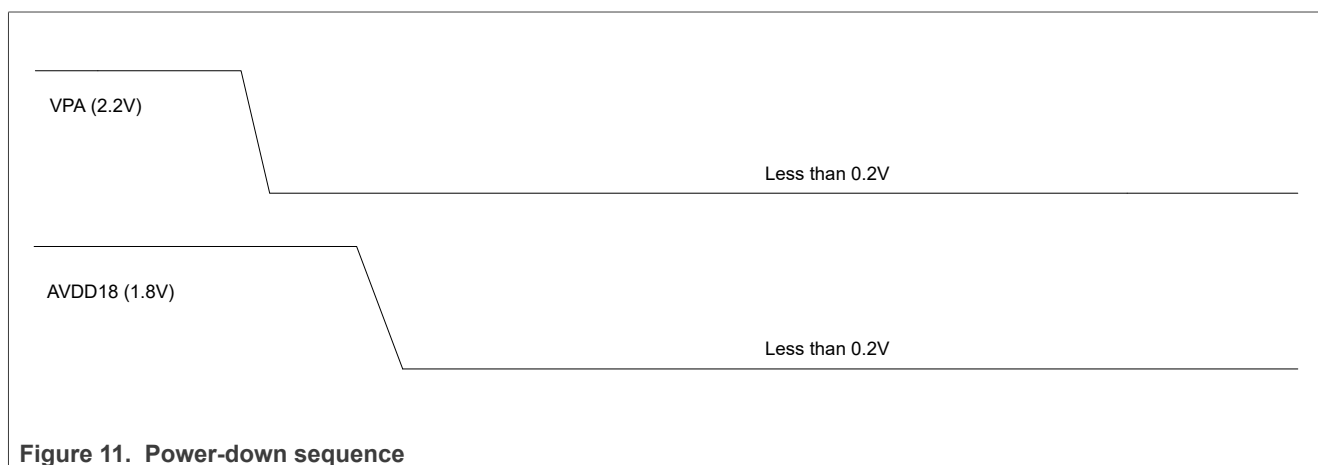
## 6.2 Power-down sequence

It is recommended:

- To ramp down AVDD18 after VPA ramps down
- To discharge all of the power supplies to less than 0.2V to reduce leakage.

PDn must be asserted when powering down the device.

[Figure 11](#) shows the power-down sequence.



## 6.3 Reset

88W8987 is reset to its default operating state under any of the following conditions:

- Internal Power-On Reset (POR): POR is triggered when the device receives power and VCORE and AVDD18 supplies are good. See [Section 6.1 "Power-up sequence"](#).
- Software/Firmware reset: the software or firmware issues a reset.
- External PDn pin assertion: the device is reset when the PDn input pin is <0.2V and transitions from low to high.

See [Section 9.10 "Power-down \(PDn\) pin specifications"](#) for the electrical specifications.

### 6.3.1 Lowest power state

The device can be put into the lowest power mode of operation to conserve energy when Wi-Fi and Bluetooth are not in use.

To put the device in the lowest power mode, assert PDn low to enter power-down mode. Once PDn is de-asserted, the power sequence must be followed. If the firmware is not downloaded, the device must be kept in power-down mode to reduce leakage.

## 7 Absolute maximum ratings

**CAUTION:** The absolute maximum ratings table defines the limitations for electrical and thermal stresses. These limits prevent permanent damage to the device. Exposure to conditions at or beyond these ratings is not guaranteed and can damage the device.

**Table 18. Absolute maximum ratings**

| Symbol               | Parameter                          | Min | Max                | Units |
|----------------------|------------------------------------|-----|--------------------|-------|
| VCORE                | 1.10V core power supply            | --  | 1.21               | V     |
| VIO                  | 1.8V/3.3V digital I/O power supply | --  | 2.2 <sup>[1]</sup> | V     |
|                      |                                    | --  | 4.0 <sup>[2]</sup> | V     |
| VIO_SD               | 1.8V digital I/O SDIO power supply | --  | 2.2                | V     |
| VIO_RF               | 1.8V/3.3V I/O power supply         | --  | 2.2 <sup>[3]</sup> | V     |
|                      |                                    | --  | 4.0 <sup>[4]</sup> | V     |
| AVDD18               | 1.8V analog power supply           | --  | 1.98               | V     |
| VPA                  | 2.2V analog power supply           | --  | 2.3                | V     |
| T <sub>STORAGE</sub> | Storage Temperature                | -55 | +125               | °C    |

[1] When using 1.8V digital I/O power supply

[2] When using 3.3V digital I/O power supply

[3] When using 1.8V I/O power supply

[4] When using 3.3V I/O power supply

**Table 19. Limiting values - QFN option**

| Symbol           | Parameter               | Condition                                 | Min  | Max  | Unit |
|------------------|-------------------------|-------------------------------------------|------|------|------|
| V <sub>ESD</sub> | Electrostatic discharge | human body model (HBM) <sup>[1]</sup>     | -1.5 | +1.5 | kV   |
|                  |                         | charged device model (CDM) <sup>[2]</sup> | -500 | +500 | V    |

[1] According to ANSI/ESDA/JEDEC JS-001.

[2] According to ANSI/ESDA/JEDEC JS-002

**Table 20. Limiting values - eWLP option**

| Symbol           | Parameter               | Condition                                 | Min  | Max  | Unit |
|------------------|-------------------------|-------------------------------------------|------|------|------|
| V <sub>ESD</sub> | Electrostatic discharge | human body model (HBM) <sup>[1]</sup>     | -1.5 | +1.5 | kV   |
|                  |                         | charged device model (CDM) <sup>[2]</sup> | -400 | +400 | V    |

[1] According to ANSI/ESDA/JEDEC JS-001.

[2] According to ANSI/ESDA/JEDEC JS-002

## 8 Recommended operating conditions

**Note:** Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

Table 21. Recommended operating conditions

| Symbol         | Parameter                          | Condition  | Min  | Typ  | Max  | Units |
|----------------|------------------------------------|------------|------|------|------|-------|
| VCORE          | 1.10V core power supply            | --         | 1.05 | 1.10 | 1.15 | V     |
| VIO            | 1.8V/3.3V digital I/O power supply | --         | 1.67 | 1.8  | 1.92 | V     |
|                |                                    |            | 3.07 | 3.3  | 3.53 | V     |
| VIO_SD         | 1.8V digital I/O SDIO power supply | --         | 1.67 | 1.8  | 1.92 | V     |
| VIO_RF         | 1.8V/3.3V I/O power supply         | --         | 1.67 | 1.8  | 1.92 | V     |
|                |                                    |            | 3.07 | 3.3  | 3.53 | V     |
| AVDD18         | 1.8V analog power supply           | --         | 1.71 | 1.8  | 1.89 | V     |
| VPA            | 2.2V analog power supply           | --         | 2.09 | 2.2  | 2.26 | V     |
| T <sub>A</sub> | Ambient operating temperature      | Extended   | -30  | --   | 85   | °C    |
|                |                                    | Industrial | -40  | --   | 85   | °C    |
| T <sub>J</sub> | Maximum junction temperature       | --         | --   | --   | 125  | °C    |

## 9 Electrical specifications

### 9.1 GPIO/LED interface specifications

#### 9.1.1 VIO DC characteristics

##### 9.1.1.1 1.8V operation

Table 22. DC electrical characteristics—1.8V operation (VIO)

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol           | Parameter           | Condition | Min     | Typ | Max     | Unit |
|------------------|---------------------|-----------|---------|-----|---------|------|
| V <sub>IH</sub>  | Input high voltage  | --        | 0.7*VIO | --  | VIO+0.4 | V    |
| V <sub>IL</sub>  | Input low voltage   | --        | -0.4    | --  | 0.3*VIO | V    |
| V <sub>HYS</sub> | Input hysteresis    | --        | 100     | --  | --      | mV   |
| V <sub>OH</sub>  | Output high voltage | --        | VIO-0.4 | --  | --      | V    |
| V <sub>OL</sub>  | Output low voltage  | --        | --      | --  | 0.4     | V    |

##### 9.1.1.2 3.3V operation

Table 23. DC electrical characteristics—3.3V operation (VIO)

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol           | Parameter           | Condition | Min     | Typ | Max     | Unit |
|------------------|---------------------|-----------|---------|-----|---------|------|
| V <sub>IH</sub>  | Input high voltage  | --        | 0.7*VIO | --  | VIO+0.4 | V    |
| V <sub>IL</sub>  | Input low voltage   | --        | -0.4    | --  | 0.3*VIO | V    |
| V <sub>HYS</sub> | Input hysteresis    | --        | 100     | --  | --      | mV   |
| V <sub>OH</sub>  | Output high voltage | --        | VIO-0.4 | --  | --      | V    |
| V <sub>OL</sub>  | Output low voltage  | --        | --      | --  | 0.4     | V    |

#### 9.1.2 LED mode

Table 24. LED mode data

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol          | Parameter              | Condition                                   | Typ                        | Unit |
|-----------------|------------------------|---------------------------------------------|----------------------------|------|
| I <sub>OH</sub> | Switching current high | Tristate on pad (requires pull-up on board) | Tristate when driving high | mA   |
| I <sub>OL</sub> | Switching current low  | @ 0.4V                                      | 10                         | mA   |

## 9.2 RF front-end control interface specifications

### 9.2.1 VIO\_RF DC characteristics

#### 9.2.1.1 1.8V operation

**Table 25. DC electrical characteristics—1.8V operation (VIO\_RF)**

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol           | Parameter           | Condition | Min        | Typ | Max        | Unit |
|------------------|---------------------|-----------|------------|-----|------------|------|
| V <sub>IH</sub>  | Input high voltage  | --        | 0.7*VIO_RF | --  | VIO_RF+0.4 | V    |
| V <sub>IL</sub>  | Input low voltage   | --        | -0.4       | --  | 0.3*VIO_RF | V    |
| V <sub>HYS</sub> | Input hysteresis    | --        | 100        | --  | --         | mV   |
| V <sub>OH</sub>  | Output high voltage | --        | VIO_RF-0.4 | --  | --         | V    |
| V <sub>OL</sub>  | Output low voltage  | --        | --         | --  | 0.4        | V    |

#### 9.2.1.2 3.3V operation

**Table 26. DC electrical characteristics—3.3V operation (VIO\_RF)**

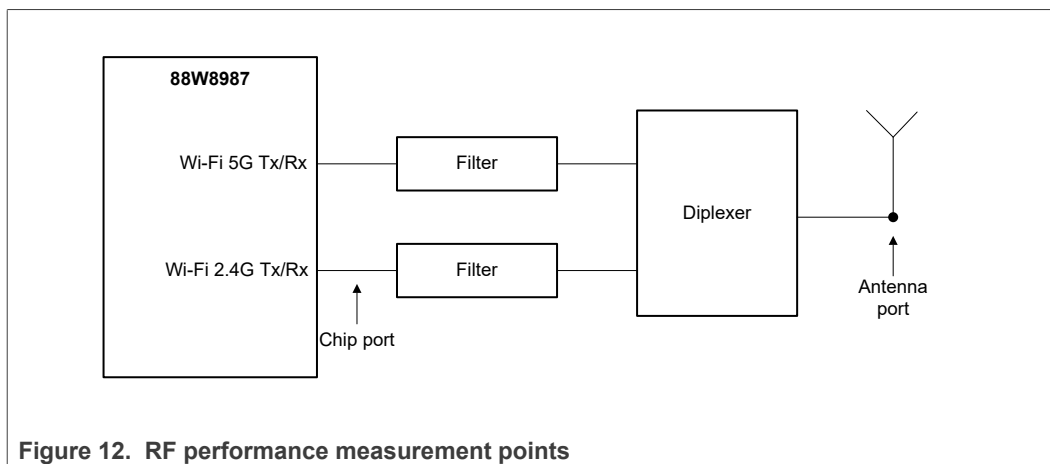
Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol           | Parameter           | Condition | Min        | Typ | Max        | Unit |
|------------------|---------------------|-----------|------------|-----|------------|------|
| V <sub>IH</sub>  | Input high voltage  | --        | 0.7*VIO_RF | --  | VIO_RF+0.4 | V    |
| V <sub>IL</sub>  | Input low voltage   | --        | -0.4       | --  | 0.3*VIO_RF | V    |
| V <sub>HYS</sub> | Input hysteresis    | --        | 100        | --  | --         | mV   |
| V <sub>OH</sub>  | Output high voltage | --        | VIO_RF-0.4 | --  | --         | V    |
| V <sub>OL</sub>  | Output low voltage  | --        | --         | --  | 0.4        | V    |

### 9.3 Wi-Fi radio specifications

#### 9.3.1 Wi-Fi radio performance measurement

The Wi-Fi transmit/receive performance is measured either at the antenna port or at the chip port.



## 9.3.2 2.4 GHz Wi-Fi receiver performance

**Note:** Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at chip port.

Table 27. 2.4 GHz Wi-Fi receiver performance

| Parameter                                                        | Conditions                                                    | Min  | Typ                | Max  | Unit |
|------------------------------------------------------------------|---------------------------------------------------------------|------|--------------------|------|------|
| RF frequency range                                               | 20 MHz and 40 MHz bandwidths                                  | 2400 | —                  | 2500 | MHz  |
| Rx input IP3 at RF high gain (In-Band)                           | Rx input IP3 when LNA in high gain mode (24 dB) at chip input | —    | -20                | —    | dBm  |
| Maximum Rx input level                                           | Maximum Rx input level without device damage                  | —    | —                  | 2    | dBm  |
| Receiver sensitivity 802.11b                                     | 1 Mbit/s                                                      | —    | -99                | —    | dBm  |
|                                                                  | 2 Mbit/s                                                      | —    | -95                | —    | dBm  |
|                                                                  | 5.5 Mbit/s                                                    | —    | -93                | —    | dBm  |
|                                                                  | 11 Mbit/s                                                     | —    | -90                | —    | dBm  |
| Receiver sensitivity 802.11g                                     | 6 Mbit/s                                                      | —    | -89                | —    | dBm  |
|                                                                  | 9 Mbit/s                                                      | —    | -89                | —    | dBm  |
|                                                                  | 12 Mbit/s                                                     | —    | -88                | —    | dBm  |
|                                                                  | 18 Mbit/s                                                     | —    | -87                | —    | dBm  |
|                                                                  | 24 Mbit/s                                                     | —    | -85                | —    | dBm  |
|                                                                  | 36 Mbit/s                                                     | —    | -81                | —    | dBm  |
|                                                                  | 48 Mbit/s                                                     | —    | -77                | —    | dBm  |
|                                                                  | 54 Mbit/s                                                     | —    | -76 <sup>[1]</sup> | —    | dBm  |
| Receiver sensitivity 802.11n HT20 <sup>[1]</sup><br>BCC waveform | MCS0                                                          | —    | -89                | —    | dBm  |
|                                                                  | MCS1                                                          | —    | -88                | —    | dBm  |
|                                                                  | MCS2                                                          | —    | -85                | —    | dBm  |
|                                                                  | MCS3                                                          | —    | -83                | —    | dBm  |
|                                                                  | MCS4                                                          | —    | -80                | —    | dBm  |
|                                                                  | MCS5                                                          | —    | -76                | —    | dBm  |
|                                                                  | MCS6                                                          | —    | -74                | —    | dBm  |
|                                                                  | MCS7                                                          | —    | -73                | —    | dBm  |
| Receiver sensitivity 802.11n HT40 <sup>[1]</sup><br>BCC waveform | MCS0                                                          | —    | -87                | —    | dBm  |
|                                                                  | MCS1                                                          | —    | -86                | —    | dBm  |
|                                                                  | MCS2                                                          | —    | -84                | —    | dBm  |
|                                                                  | MCS3                                                          | —    | -81                | —    | dBm  |
|                                                                  | MCS4                                                          | —    | -77                | —    | dBm  |
|                                                                  | MCS5                                                          | —    | -73                | —    | dBm  |
|                                                                  | MCS6                                                          | —    | -72                | —    | dBm  |
|                                                                  | MCS7                                                          | —    | -71                | —    | dBm  |

Table 27. 2.4 GHz Wi-Fi receiver performance...continued

| Parameter                                                             | Conditions     | Min | Typ | Max | Unit |
|-----------------------------------------------------------------------|----------------|-----|-----|-----|------|
| Receiver maximum input level                                          | 802.11b        | —   | -1  | —   | dBm  |
|                                                                       | 802.11g        | —   | -2  | —   | dBm  |
|                                                                       | 802.11n MCS0-4 | —   | -1  | —   | dBm  |
|                                                                       | 802.11n MCS5-6 | —   | -2  | —   | dBm  |
|                                                                       | 802.11n MCS7   | —   | -5  | —   | dBm  |
| Receiver adjacent channel interference rejection (ACI) 802.11b        | 1 Mbit/s       | —   | 54  | —   | dB   |
|                                                                       | 2 Mbit/s       | —   | 49  | —   | dB   |
|                                                                       | 5.5 Mbit/s     | —   | 47  | —   | dB   |
|                                                                       | 11 Mbit/s      | —   | 45  | —   | dB   |
| Receiver adjacent channel interference rejection (ACI) 802.11g        | 6 Mbit/s       | —   | 37  | —   | dB   |
|                                                                       | 9 Mbit/s       | —   | 35  | —   | dB   |
|                                                                       | 12 Mbit/s      | —   | 39  | —   | dB   |
|                                                                       | 18 Mbit/s      | —   | 36  | —   | dB   |
|                                                                       | 24 Mbit/s      | —   | 33  | —   | dB   |
|                                                                       | 36 Mbit/s      | —   | 27  | —   | dB   |
|                                                                       | 48 Mbit/s      | —   | 27  | —   | dB   |
|                                                                       | 54 Mbit/s      | —   | 24  | —   | dB   |
| Receiver adjacent channel interference rejection (ACI) 802.11n, HT20  | MCS0           | —   | 37  | —   | dB   |
|                                                                       | MCS1           | —   | 36  | —   | dB   |
|                                                                       | MCS2           | —   | 36  | —   | dB   |
|                                                                       | MCS3           | —   | 30  | —   | dB   |
|                                                                       | MCS4           | —   | 28  | —   | dB   |
|                                                                       | MCS5           | —   | 26  | —   | dB   |
|                                                                       | MCS6           | —   | 21  | —   | dB   |
|                                                                       | MCS7           | —   | 20  | —   | dB   |
| Receiver adjacent channel interference rejection (ACI) 802.11n, HT40, | MCS0           | —   | 33  | —   | dB   |
|                                                                       | MCS1           | —   | 32  | —   | dB   |
|                                                                       | MCS2           | —   | 29  | —   | dB   |
|                                                                       | MCS3           | —   | 27  | —   | dB   |
|                                                                       | MCS4           | —   | 26  | —   | dB   |
|                                                                       | MCS5           | —   | 22  | —   | dB   |
|                                                                       | MCS6           | —   | 19  | —   | dB   |
|                                                                       | MCS7           | —   | 17  | —   | dB   |

[1] De-sense of ~2 dB at 2472 MHz

### 9.3.3 5 GHz Wi-Fi receiver performance

**Note:** Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at the chip port.

Table 28. 5 GHz Wi-Fi receiver performance

| Parameter                                      | Conditions                                                    | Min  | Typ | Max  | Unit |
|------------------------------------------------|---------------------------------------------------------------|------|-----|------|------|
| RF frequency range                             | 5 GHz—IEEE 802.11ac/n/a                                       | 4900 | --  | 5925 | MHz  |
| Rx input IP3 at RF high gain (In-Band)         | Rx Input IP3 when LNA in high gain mode (24 dB) at chip input | —    | -20 | —    | dBm  |
| Maximum Rx input level                         | Maximum Rx input level without device damage                  | —    | —   | 2    | dBm  |
| Receiver sensitivity 802.11a                   | 6 Mbit/s                                                      | --   | -92 | --   | dBm  |
|                                                | 9 Mbit/s                                                      | --   | -92 | --   | dBm  |
|                                                | 12 Mbit/s                                                     | --   | -91 | --   | dBm  |
|                                                | 18 Mbit/s                                                     | --   | -89 | --   | dBm  |
|                                                | 24 Mbit/s                                                     | --   | -86 | --   | dBm  |
|                                                | 36 Mbit/s                                                     | --   | -83 | --   | dBm  |
|                                                | 48 Mbit/s                                                     | --   | -78 | --   | dBm  |
|                                                | 54 Mbit/s                                                     | --   | -77 | --   | dBm  |
| Receiver sensitivity 802.11n HT20 BCC waveform | MCS0                                                          | --   | -92 | --   | dBm  |
|                                                | MCS1                                                          | --   | -90 | --   | dBm  |
|                                                | MCS2                                                          | --   | -87 | --   | dBm  |
|                                                | MCS3                                                          | --   | -84 | --   | dBm  |
|                                                | MCS4                                                          | --   | -81 | --   | dBm  |
|                                                | MCS5                                                          | --   | -76 | --   | dBm  |
|                                                | MCS6                                                          | --   | -75 | --   | dBm  |
|                                                | MCS7                                                          | --   | -73 | --   | dBm  |
| Receiver sensitivity 802.11n HT40 BCC waveform | MCS0                                                          | --   | -88 | --   | dBm  |
|                                                | MCS1                                                          | --   | -87 | --   | dBm  |
|                                                | MCS2                                                          | --   | -84 | --   | dBm  |
|                                                | MCS3                                                          | --   | -81 | --   | dBm  |
|                                                | MCS4                                                          | --   | -78 | --   | dBm  |
|                                                | MCS5                                                          | --   | -74 | --   | dBm  |
|                                                | MCS6                                                          | --   | -73 | --   | dBm  |
|                                                | MCS7                                                          | --   | -71 | --   | dBm  |

Table 28. 5 GHz Wi-Fi receiver performance...continued

| Parameter                                        | Conditions           | Min | Typ | Max | Unit |
|--------------------------------------------------|----------------------|-----|-----|-----|------|
| Receiver sensitivity 802.11ac VHT20 BCC waveform | MCS0                 | --  | -92 | --  | dBm  |
|                                                  | MCS1                 | --  | -90 | --  | dBm  |
|                                                  | MCS2                 | --  | -88 | --  | dBm  |
|                                                  | MCS3                 | --  | -85 | --  | dBm  |
|                                                  | MCS4                 | --  | -83 | --  | dBm  |
|                                                  | MCS5                 | --  | -80 | --  | dBm  |
|                                                  | MCS6                 | --  | -78 | --  | dBm  |
|                                                  | MCS7                 | --  | -76 | --  | dBm  |
|                                                  | MCS8                 | --  | -72 | --  | dBm  |
| Receiver sensitivity 802.11ac VHT40 BCC waveform | MCS0                 | --  | -88 | --  | dBm  |
|                                                  | MCS1                 | --  | -87 | --  | dBm  |
|                                                  | MCS2                 | --  | -85 | --  | dBm  |
|                                                  | MCS3                 | --  | -82 | --  | dBm  |
|                                                  | MCS4                 | --  | -80 | --  | dBm  |
|                                                  | MCS5                 | --  | -76 | --  | dBm  |
|                                                  | MCS6                 | --  | -75 | --  | dBm  |
|                                                  | MCS7                 | --  | -74 | --  | dBm  |
|                                                  | MCS8                 | --  | -70 | --  | dBm  |
|                                                  | MCS9                 | --  | -68 | --  | dBm  |
| Receiver sensitivity 802.11ac VHT80 BCC waveform | MCS0                 | --  | -84 | --  | dBm  |
|                                                  | MCS1                 | --  | -84 | --  | dBm  |
|                                                  | MCS2                 | --  | -82 | --  | dBm  |
|                                                  | MCS3                 | --  | -79 | --  | dBm  |
|                                                  | MCS4                 | --  | -78 | --  | dBm  |
|                                                  | MCS5                 | --  | -73 | --  | dBm  |
|                                                  | MCS6                 | --  | -72 | --  | dBm  |
|                                                  | MCS7                 | --  | -71 | --  | dBm  |
|                                                  | MCS8                 | --  | -66 | --  | dBm  |
|                                                  | MCS9                 | --  | -64 | --  | dBm  |
| Receiver maximum input level                     | 802.11a 6-36 Mbit/s  | --  | -3  | --  | dBm  |
|                                                  | 802.11a 48-54 Mbit/s | --  | -5  | --  | dBm  |
|                                                  | 802.11n MCS0-4       | --  | -3  | --  | dBm  |
|                                                  | 802.11n MCS5         | --  | -4  | --  | dBm  |
|                                                  | 802.11n MCS6         | --  | -5  | --  | dBm  |
|                                                  | 802.11n MCS7-9       | --  | -8  | --  | dBm  |

Table 28. 5 GHz Wi-Fi receiver performance...continued

| Parameter                                                            | Conditions | Min | Typ | Max | Unit |
|----------------------------------------------------------------------|------------|-----|-----|-----|------|
| Receiver adjacent channel interference rejection (ACI) 802.11a       | 6 Mbit/s   | --  | 34  | --  | dB   |
|                                                                      | 9 Mbit/s   | --  | 32  | --  | dB   |
|                                                                      | 12 Mbit/s  | --  | 33  | --  | dB   |
|                                                                      | 18 Mbit/s  | --  | 32  | --  | dB   |
|                                                                      | 24 Mbit/s  | --  | 29  | --  | dB   |
|                                                                      | 36 Mbit/s  | --  | 24  | --  | dB   |
|                                                                      | 48 Mbit/s  | --  | 24  | --  | dB   |
|                                                                      | 54 Mbit/s  | --  | 17  | --  | dB   |
| Receiver adjacent channel interference rejection (ACI) 802.11n, HT20 | MCS0       | --  | 32  | --  | dB   |
|                                                                      | MCS1       | --  | 31  | --  | dB   |
|                                                                      | MCS2       | --  | 31  | --  | dB   |
|                                                                      | MCS3       | --  | 26  | --  | dB   |
|                                                                      | MCS4       | --  | 22  | --  | dB   |
|                                                                      | MCS5       | --  | 20  | --  | dB   |
|                                                                      | MCS6       | --  | 17  | --  | dB   |
|                                                                      | MCS7       | --  | 15  | --  | dB   |
| Receiver adjacent channel interference rejection (ACI) 802.11n, HT40 | MCS0       | --  | 29  | --  | dB   |
|                                                                      | MCS1       | --  | 28  | --  | dB   |
|                                                                      | MCS2       | --  | 28  | --  | dB   |
|                                                                      | MCS3       | --  | 22  | --  | dB   |
|                                                                      | MCS4       | --  | 23  | --  | dB   |
|                                                                      | MCS5       | --  | 19  | --  | dB   |
|                                                                      | MCS6       | --  | 18  | --  | dB   |
|                                                                      | MCS7       | --  | 16  | --  | dB   |

## 9.3.4 2.4 GHz Wi-Fi transmitter performance

**Note:** Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at the chip port.

Table 29. 2.4 GHz Wi-Fi transmitter performance

| Parameter                                      | Conditions                                                   | Min  | Typ               | Max  | Unit |
|------------------------------------------------|--------------------------------------------------------------|------|-------------------|------|------|
| RF frequency range                             | 2.4 GHz—IEEE 802.11n/g/b                                     | 2400 | —                 | 2500 | MHz  |
|                                                | 2.4 GHz—IEEE 802.11ac, bandwidth 20 MHz and bandwidth 40 MHz |      |                   |      |      |
| Transmitter output saturation                  | Saturation power at chip output                              | —    | 27                | —    | dBm  |
| Transmit carrier suppression (CW)              | Carrier suppression at chip output                           | —    | -36               | —    | dB   |
| Transmit I/Q suppression with IQ calibration   | I/Q suppression at chip output                               | —    | -45               | —    | dBc  |
| Transmit power (EVM and mask compliant) 20 MHz | 802.11b                                                      | —    | 22                | —    | dBm  |
|                                                | OFDM BPSK                                                    | —    | 21                | —    | dBm  |
|                                                | OFDM QPSK                                                    | —    | 21                | —    | dBm  |
|                                                | OFDM 16-QAM                                                  | —    | 21                | —    | dBm  |
|                                                | OFDM 64-QAM                                                  | —    | 21                | —    | dBm  |
| Transmit power (EVM and mask compliant) 40 MHz | OFDM BPSK                                                    | —    | 20                | —    | dBm  |
|                                                | OFDM QPSK                                                    | —    | 20                | —    | dBm  |
|                                                | OFDM 16-QAM                                                  | —    | 20                | —    | dBm  |
|                                                | OFDM 64-QAM                                                  | —    | 20                | —    | dBm  |
| Transmit output power level control range      | —                                                            | —    | 22 <sup>[1]</sup> | —    | dB   |
| Transmit output power control step             | —                                                            | —    | 1 <sup>[2]</sup>  | —    | dB   |
| Transmit output power accuracy                 | —                                                            | —    | ±1.5              | —    | dB   |
| Transmit carrier suppression                   | 802.11n HT40 MCS7 at 18 dBm                                  | —    | 49                | —    | dB   |

[1] 0-22 dBm

[2] Hardware capability = 0.5 dB, software capability = 1 dB

### 9.3.5 5 GHz Wi-Fi transmitter performance

**Note:** Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at the chip port.

Table 30. 5 GHz Wi-Fi transmitter performance

| Parameter                                      | Conditions                         | Min  | Typ               | Max  | Unit |
|------------------------------------------------|------------------------------------|------|-------------------|------|------|
| RF frequency range                             | 5 GHz—IEEE 802.11ac/n/a            | 4900 | —                 | 5925 | MHz  |
| Transmit output saturation                     | Saturation power at chip output    | —    | 27                | —    | dBm  |
| Transmit carrier suppression (CW)              | Carrier suppression at chip output | —    | -36               | —    | dB   |
| Transmit I/Q suppression with IQ calibration   | I/Q suppression at chip output     | —    | -45               | —    | dBc  |
| Transmit power (EVM and mask compliant) 20 MHz | OFDM BPSK                          | —    | 21                | —    | dBm  |
|                                                | OFDM QPSK                          | —    | 21                | —    | dBm  |
|                                                | OFDM 16-QAM                        | —    | 21                | —    | dBm  |
|                                                | OFDM 64-QAM (MCS7)                 | —    | 21                | —    | dBm  |
|                                                | OFDM 256-QAM (MCS8)                | —    | 20                | —    | dBm  |
| Transmit power (EVM and mask compliant) 40 MHz | OFDM BPSK                          | —    | 20                | —    | dBm  |
|                                                | OFDM QPSK                          | —    | 20                | —    | dBm  |
|                                                | OFDM 16-QAM                        | —    | 20                | —    | dBm  |
|                                                | OFDM 64-QAM (MCS7)                 | —    | 20                | —    | dBm  |
|                                                | OFDM 256-QAM (MCS9)                | —    | 18                | —    | dBm  |
| Transmit power (EVM and mask compliant) 80 MHz | OFDM BPSK                          | —    | 17                | —    | dBm  |
|                                                | OFDM QPSK                          | —    | 17                | —    | dBm  |
|                                                | OFDM 16-QAM                        | —    | 17                | —    | dBm  |
|                                                | OFDM 64-QAM (MCS7)                 | —    | 17                | —    | dBm  |
|                                                | OFDM 256-QAM (MCS9)                | —    | 15                | —    | dBm  |
| Transmit output power level control range      |                                    | —    | 21 <sup>[1]</sup> | —    | dB   |
| Transmit output power control step             |                                    | —    | 1 <sup>[2]</sup>  | —    | dB   |
| Transmit output power accuracy                 |                                    | —    | ±1.5              | —    | dB   |
| Transmit carrier suppression                   | 802.11ac MCS9 VHT80, at 15 dBm     | —    | 51                | —    | dBc  |

[1] 0-21 dBm

[2] Hardware capability = 0.5 dB, software capability = 1 dB

### 9.3.6 Local oscillator

**Table 31. Local oscillator**

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Parameter                                                    | Condition                                      | Min  | Typ  | Max | Units   |
|--------------------------------------------------------------|------------------------------------------------|------|------|-----|---------|
| Phase noise                                                  | Measured at 2.438 GHz at 100 kHz offset        | —    | -103 | —   | dBc/Hz  |
| Phase noise                                                  | Measured at 5.501 GHz at 100 kHz offset        | —    | -100 | —   | dBc/Hz  |
| Integrated RMS phase noise at RF output (from 1 kHz–10 MHz)  | Reference clock frequency = 38.4 MHz (2.4 GHz) | —    | 0.3  | —   | degrees |
| Integrated RMS phase noise at RF output (from 10 kHz–10 MHz) | Reference clock frequency = 38.4 MHz (5 GHz)   | —    | 0.5  | —   | degrees |
| Frequency resolution                                         | —                                              | 0.02 | —    | —   | kHz     |

## 9.4 Bluetooth radio specifications

The Bluetooth radio interface pin is powered by AVDD18 voltage supply.

### 9.4.1 Bluetooth and Bluetooth LE receiver performance

**Note:** Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at BRF\_ANT pin.

Table 32. Bluetooth and Bluetooth LE receiver performance

| Parameter                           | Conditions                            | Min | Typ   | Max | Unit |
|-------------------------------------|---------------------------------------|-----|-------|-----|------|
| RF frequency range                  | —                                     | 2.4 | —     | 2.5 | GHz  |
| IF frequency                        | —                                     | —   | 2     | —   | MHz  |
| Input IP3 (@ maximum gain of 72 dB) | —                                     | —   | -19   | —   | dBm  |
| In-band blocking                    | <b>GFSK</b><br>C/I (Co-channel)       | —   | 10    | —   | dB   |
|                                     | C/I (1 MHz)                           | —   | -4    | —   | dB   |
|                                     | C/I (2 MHz)                           | —   | -45   | —   | dB   |
|                                     | C/I (3 MHz)                           | —   | -49   | —   | dB   |
|                                     | C/I (Image)                           | —   | -21   | —   | dB   |
|                                     | C/I (Image ±1 MHz)                    | —   | -32   | —   | dB   |
|                                     | <b>Pi/4-DQPSK</b><br>C/I (Co-channel) | —   | 10    | —   | dB   |
|                                     | C/I (1 MHz)                           | —   | -9    | —   | dB   |
|                                     | C/I (2 MHz)                           | —   | -47   | —   | dB   |
|                                     | C/I (3 MHz)                           | —   | -51   | —   | dB   |
|                                     | C/I (Image)                           | —   | -19   | —   | dB   |
|                                     | C/I (Image ±1 MHz)                    | —   | -35   | —   | dB   |
|                                     | <b>8-DPSK</b><br>C/I (Co-channel)     | —   | 16    | —   | dB   |
|                                     | C/I (1 MHz)                           | —   | -6    | —   | dB   |
|                                     | C/I (2 MHz)                           | —   | -42   | —   | dB   |
|                                     | C/I (3 MHz)                           | —   | -48   | —   | dB   |
|                                     | C/I (Image)                           | —   | -12   | —   | dB   |
|                                     | C/I (Image ±1 MHz)                    | —   | -33   | —   | dB   |
| Out-of-band blocking                | 30–2000 MHz                           | —   | -12.5 | —   | dBm  |
|                                     | 2–2.399 GHz                           | —   | -12.4 | —   | dBm  |
|                                     | 2.484–3 GHz                           | —   | -18   | —   | dBm  |
|                                     | 3–12.75 GHz                           | —   | -2.6  | —   | dBm  |
| RSSI range                          | Resolution = 1 dB                     | —   | -90   | 0   | dBm  |
| 50 Ω return loss                    | —                                     | —   | —     | -10 | dB   |

Table 32. Bluetooth and Bluetooth LE receiver performance...continued

| Parameter                                                       | Conditions            | Min | Typ                | Max | Unit |
|-----------------------------------------------------------------|-----------------------|-----|--------------------|-----|------|
| Bluetooth sensitivity (RCV/CA/01/C & RCV/CA/02/C & RCV/CA/07/C) | DH5                   | —   | -96 <sup>[1]</sup> | —   | dBm  |
|                                                                 | 2DH5                  | —   | -95 <sup>[2]</sup> | —   | dBm  |
|                                                                 | 3DH5                  | —   | -88 <sup>[3]</sup> | —   | dBm  |
| Bluetooth LE sensitivity (RCV-LE/CA/02/C)                       | Bluetooth LE 1 Mbit/s | —   | -99 <sup>[4]</sup> | —   | dBm  |
|                                                                 | Bluetooth LE 2 Mbit/s | —   | -96 <sup>[4]</sup> | —   | dBm  |

[1] Desense of ~9.5 dB at CH 2419 MHz, ~6 dB at 2457 MHz, ~9 dB at 2458 MHz due to internal clock harmonics

[2] Desense of ~8.5 dB at CH 2419 MHz, ~3 dB at CH 2432 MHz, ~5 dB at 2457 MHz, ~7.5 dB at 2458 MHz due to internal clock harmonics

[3] Desense of ~9 dB at CH 2419 MHz, ~3.5dB at CH 2432 MHz, ~4.5 dB at 2457 MHz, ~7.5 dB at 2458 MHz due to internal clock harmonics

[4] Desense of ~7 dB at CH 2432 MHz and ~9 dB at 2458MHz due to internal clock harmonics

### 9.4.2 Bluetooth and Bluetooth LE transmitter performance

**Note:** Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at BRF\_ANT pin.

Table 33. Bluetooth and Bluetooth LE transmitter

| Parameter                                   | Conditions                                                                                                                                          | Min | Typ    | Max    | Unit   |
|---------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-----|--------|--------|--------|
| RF frequency range                          | —                                                                                                                                                   | 2.4 | —      | 2.5    | GHz    |
| Gain range                                  | Class 1 without external PA                                                                                                                         | —   | 30     | —      | dB     |
| Gain resolution                             | —                                                                                                                                                   | —   | 0.5    | —      | dB     |
| Spurious emission (BDR) (in-band)           | ±500 kHz                                                                                                                                            | —   | —      | -20    | dBc    |
|                                             | ±2 MHz                                                                                                                                              | —   | -33    | -20    | dBm    |
|                                             | ±3 MHz                                                                                                                                              | —   | -45    | -40    | dBm    |
| Spurious emission (EDR) (in-band)           | ±1 MHz                                                                                                                                              | —   | —      | -26    | dBc    |
|                                             | ±1.5 MHz                                                                                                                                            | —   | —      | -20    | dBm    |
|                                             | ±2.5 MHz                                                                                                                                            | —   | —      | -40    | dBm    |
| Spurious emission (out-of-band)             | 30–88 MHz                                                                                                                                           | —   | -65    | -41.25 | dBm    |
|                                             | 88–960 MHz                                                                                                                                          | —   | -65    | -41.25 |        |
|                                             | 0.96–20 GHz<br>All frequencies in this range < -41.25 dBm,<br>except at 2x Bluetooth channel frequency.<br>Measured at pin without external filter. | —   | -35    | -25    |        |
|                                             | Restricted—2.38–2.39 GHz                                                                                                                            | —   | -55    | -41.25 |        |
|                                             | Restricted—2.4835–2.6 GHz                                                                                                                           | —   | -50    | -41.25 |        |
| Out-of-band/<br>Cellular band noise         | GSM850 (869–894 MHz)                                                                                                                                | —   | -140   | —      | dBm/Hz |
|                                             | GSM900 (925–960 MHz)                                                                                                                                | —   | -140   | —      |        |
|                                             | GSM DCS (1805–1880 MHz)                                                                                                                             | —   | -135   | —      |        |
|                                             | GSM PCS (1930–1990 MHz)                                                                                                                             | —   | -135   | —      |        |
|                                             | GPS (1575.42 ±1.023 MHz)                                                                                                                            | —   | -140   | —      |        |
|                                             | WCDMA Band I (2110–2170 MHz)                                                                                                                        | —   | -130   | —      |        |
|                                             | WCDMA Band V (869–894 MHz)                                                                                                                          | —   | -140   | —      |        |
| Transmit output power<br>(TRM/CA/01/C)      | BDR                                                                                                                                                 | —   | 13     | —      | dBm    |
|                                             | EDR                                                                                                                                                 | —   | 10     | —      | dBm    |
| Transmit output power accuracy              | —                                                                                                                                                   | —   | ±1.5   | —      | dB     |
| Power control (TRM/CA/03/C)                 | —                                                                                                                                                   | —   | 5      | —      | dB     |
| Frequency range (TRM/CA/04/C)               | Freq Low                                                                                                                                            | —   | 2400.9 | —      | MHz    |
|                                             | Freq High                                                                                                                                           | —   | 2481   | —      | MHz    |
| -20dB BW (TRM/CA/05/C)                      | DH5                                                                                                                                                 | —   | 955    | —      | kHz    |
| Modulation characteristics<br>(TRM/CA/07/C) | Delta F1 avg                                                                                                                                        | —   | 164    | —      | kHz    |
|                                             | Delta F2 max Threshold                                                                                                                              | —   | 100    | —      | %      |

Table 33. Bluetooth and Bluetooth LE transmitter...continued

| Parameter                                                             | Conditions                               | Min | Typ  | Max | Unit |
|-----------------------------------------------------------------------|------------------------------------------|-----|------|-----|------|
| Modulation characteristics (TRM/CA/07/C)                              | Delta F2/Delta F1                        | —   | 0.9  | —   | —    |
|                                                                       | Delta F2 avg                             | —   | 148  | —   | kHz  |
| ICFT (TRM/CA/08/C)                                                    | DH1                                      | —   | 19   | —   | kHz  |
| Carrier frequency drift (TRM/CA/09/C)                                 | Max Drift - DH1                          | —   | -7   | —   | kHz  |
|                                                                       | Drift Rate - DH1                         | —   | -0.9 | —   | kHz  |
|                                                                       | Max Drift - DH3                          | —   | -7   | —   | kHz  |
|                                                                       | Drift Rate - DH3                         | —   | -1   | —   | kHz  |
|                                                                       | Max Drift - DH5                          | —   | -7   | —   | kHz  |
|                                                                       | Drift Rate - DH5                         | —   | -1.3 | —   | kHz  |
| EDR relative power (TRM/CA/10/C)                                      | 2DH5 (DPSK/GFSK)                         | —   | -0.1 | —   | dB   |
|                                                                       | 3DH5 (DPSK/GFSK)                         | —   | -0.1 | —   | dB   |
| EDR carrier frequency stability and modulation accuracy (TRM/CA/11/C) | 2DH5 Peak DEVM                           | —   | 0.07 | —   | —    |
|                                                                       | 2DH5 RMS DEVM                            | —   | 0.03 | —   | —    |
|                                                                       | 3DH5 Peak DEVM                           | —   | 0.08 | —   | —    |
|                                                                       | 3DH5 RMS DEVM                            | —   | 0.03 | —   | —    |
| Diff. phase encoding (TRM/CA/12/C)                                    | 2DH5                                     | —   | 100  | —   | %    |
|                                                                       | 3DH5                                     | —   | 100  | —   | %    |
| Bluetooth LE output power (TRM/-Bluetooth LE/CA/01/C)                 | Bluetooth LE 1 Mbit/s                    | —   | 10   | —   | dBm  |
|                                                                       | Bluetooth LE 2 Mbit/s                    | —   | 10   | —   | dBm  |
| Bluetooth LE modulation characteristics (TRM-Bluetooth LE/CA/05/C)    | Delta F1 avg - Bluetooth LE 1 Mbit/s     | —   | 247  | —   | kHz  |
|                                                                       | Delta F2/Delta F1- Bluetooth LE 1 Mbit/s | —   | 0.9  | —   | kHz  |
|                                                                       | Delta F2 avg - Bluetooth LE 1 Mbit/s     | —   | 223  | —   | kHz  |
|                                                                       | Delta F1 avg - Bluetooth LE 2 Mbit/s     | —   | 504  | —   | kHz  |
|                                                                       | Delta F2/Delta F1- 2 Mbit/s              | —   | 1    | —   | kHz  |
|                                                                       | Delta F2 avg- Bluetooth LE 2 Mbit/s      | —   | 474  | —   | kHz  |
| Bluetooth LE carrier frequency drift (TRM-Bluetooth LE/CA/06/C)       | Max Drift - Bluetooth LE 1 Mbit/s        | —   | 0.5  | —   | kHz  |
|                                                                       | Drift Rate - Bluetooth LE 1 Mbit/s       | —   | 1.5  | —   | kHz  |
|                                                                       | Max Drift - Bluetooth LE 2 Mbit/s        | —   | -1.5 | —   | kHz  |
|                                                                       | Drift Rate - Bluetooth LE 2 Mbit/s       | —   | 1    | —   | kHz  |
| Frequency accuracy (TRM-LE/CA/BV-06-C)                                | Bluetooth LE 1 Mbit/s                    | —   | -9   | —   | kHz  |
|                                                                       | Bluetooth LE 2 Mbit/s                    | —   | -10  | —   | kHz  |

## 9.5 Current consumption

**Note:** Unless otherwise stated, all specifications are at 25°C, nominal voltage, across frequency and typical value with SDIO 2.0 SDR25 50 MHz clock (4-bit mode). Data is collected with SDIO-SDIO interface configuration. The transmit power level in transmit mode refers to the chip port ([Section 9.3.1](#)).

Table 34. Current consumption

| Mode                                                        | VIO_3.3 V | 2.2 V | 1.8 V | 1.1 V | Unit |
|-------------------------------------------------------------|-----------|-------|-------|-------|------|
| <b>Sleep mode current consumption</b>                       |           |       |       |       |      |
| Power down                                                  | 0.11      | 0     | 0.04  | 2.8   | mA   |
| Wi-Fi and Bluetooth in deep-sleep mode                      | 0.08      | 0     | 0.02  | 1.22  | mA   |
| Wi-Fi only in deep-sleep mode                               | 0.08      | 0     | 0.024 | 1.14  | mA   |
| Bluetooth only in deep-sleep mode                           | 0.08      | 0     | 0.025 | 1.04  | mA   |
| Bluetooth LE only in deep-sleep mode                        | 0.08      | 0     | 0.02  | 1.01  | mA   |
| <b>Bluetooth LE current consumption<sup>[1]</sup></b>       |           |       |       |       |      |
| Bluetooth LE advertise (interval = 1.28 s)                  | 0.08      | 0     | 0.05  | 1.1   | mA   |
| Bluetooth LE scan (interval = 1.28 s, window = 11.25 ms)    | 0.08      | 0     | 0.15  | 1.2   | mA   |
| Bluetooth LE link (central mode, interval=1.28 s)           | 0.08      | 0     | 0.07  | 1.2   | mA   |
| Bluetooth LE peak transmit (at 0 dBm), 1 Mbit/s             | 0.44      | 0     | 25    | 21    | mA   |
| Bluetooth LE peak transmit (at 5 dBm), 1 Mbit/s             | 0.44      | 0     | 37    | 23    | mA   |
| Bluetooth LE peak transmit (at 10 dBm), 1 Mbit/s            | 0.44      | 0     | 53    | 22    | mA   |
| Bluetooth LE peak receive, 1 Mbit/s                         | 0.44      | 0     | 17    | 21    | mA   |
| <b>Bluetooth current consumption<sup>[1]</sup></b>          |           |       |       |       |      |
| Bluetooth page scan                                         | 0.08      | 0     | 0.18  | 1.2   | mA   |
| Bluetooth page and inquiry scan                             | 0.08      | 0     | 0.32  | 1.33  | mA   |
| Bluetooth ACL link, central sniff mode, (interval = 1.28s)  | 0.08      | 0     | 0.09  | 1.3   | mA   |
| Bluetooth ACL link, central sniff mode, (interval = 500 ms) | 0.08      | 0     | 0.18  | 1.7   | mA   |
| Bluetooth ACL (data pump) DH1                               | 0.44      | 0     | 11.7  | 18    | mA   |
| Bluetooth ACL (data pump) 2-DH3                             | 0.44      | 0     | 17.2  | 19.5  | mA   |
| Bluetooth ACL (data pump) 3-DH5                             | 0.44      | 0     | 19.3  | 20    | mA   |
| Bluetooth SCO HV3 peak transmit (at 0 dBm)                  | 0.44      | 0     | 25    | 21    | mA   |
| Bluetooth SCO HV3 peak transmit (at 5 dBm)                  | 0.44      | 0     | 37    | 23    | mA   |
| Bluetooth SCO HV3 peak transmit (at 10 dBm)                 | 0.44      | 0     | 53    | 22    | mA   |
| Bluetooth SCO HV3 peak transmit (at 13 dBm)                 | 0.44      | 0     | 67    | 22    | mA   |
| Bluetooth SCO HV3 Peak Receive                              | 0.44      | 0     | 17    | 21    | mA   |
| Bluetooth peak transmit (at 0 dBm), DH5                     | 0.44      | 0     | 25    | 21    | mA   |
| Bluetooth peak transmit (at 5 dBm), DH5                     | 0.44      | 0     | 37    | 23    | mA   |
| Bluetooth peak transmit (at 10 dBm), DH5                    | 0.44      | 0     | 53    | 22    | mA   |
| Bluetooth peak transmit (at 13 dBm), DH5                    | 0.44      | 0     | 67    | 22    | mA   |

Table 34. Current consumption...continued

| Mode                                                 | VIO_3.3 V | 2.2 V | 1.8 V | 1.1 V | Unit |
|------------------------------------------------------|-----------|-------|-------|-------|------|
| Bluetooth peak receive, DH5                          | 0.44      | 0     | 17    | 21    | mA   |
| <b>IEEE power save mode<sup>[2]</sup></b>            |           |       |       |       |      |
| IEEE-PS_2GHz-Legacy (DTIM-1)                         | 0.08      | 0     | 1     | 3.18  | mA   |
| IEEE-PS_2GHz-Legacy (DTIM-3)                         | 0.08      | 0     | 0.35  | 1.88  | mA   |
| IEEE-PS_2GHz-Legacy (DTIM-5)                         | 0.08      | 0     | 0.2   | 1.7   | mA   |
| IEEE-PS_2GHz-Legacy (DTIM-10)                        | 0.08      | 0     | 0.14  | 1.27  | mA   |
| IEEE-PS_5GHz-Legacy (DTIM-1)                         | 0.08      | 0     | 0.7   | 2.33  | mA   |
| IEEE-PS_5GHz-Legacy (DTIM-3)                         | 0.08      | 0     | 0.25  | 1.6   | mA   |
| IEEE-PS_5GHz-Legacy (DTIM-5)                         | 0.08      | 0     | 0.15  | 1.43  | mA   |
| IEEE-PS_5GHz-Legacy (DTIM-10)                        | 0.08      | 0     | 0.12  | 1.32  | mA   |
| <b>2.4 GHz Wi-Fi receive idle mode<sup>[3]</sup></b> |           |       |       |       |      |
| 802.11b, 11 Mbit/s                                   | 0.41      | 0     | 44    | 87    | mA   |
| 802.11g, 54 Mbit/s                                   | 0.41      | 0     | 44    | 87    | mA   |
| 802.11n, HT20 MCS7                                   | 0.41      | 0     | 44    | 87    | mA   |
| <b>2.4 GHz Wi-Fi receive mode<sup>[3]</sup></b>      |           |       |       |       |      |
| 802.11b, 11 Mbit/s                                   | 0.41      | 0     | 40    | 95    | mA   |
| 802.11g, 54 Mbit/s                                   | 0.41      | 0     | 38    | 112   | mA   |
| 802.11n, HT20 MCS7                                   | 0.41      | 0     | 38    | 118   | mA   |
| <b>5 GHz Wi-Fi 5 receive idle mode<sup>[3]</sup></b> |           |       |       |       |      |
| 802.11a, 54 Mbit/s                                   | 0.41      | 0     | 62    | 95    | mA   |
| 802.11n, HT20 MCS7                                   | 0.41      | 0     | 64    | 95    | mA   |
| 802.11n, HT40 MCS7                                   | 0.41      | 0     | 76    | 100   | mA   |
| 802.11ac, VHT20 MCS8                                 | 0.41      | 0     | 64    | 95    | mA   |
| 802.11ac, VHT40 MCS9                                 | 0.41      | 0     | 76    | 100   | mA   |
| 802.11ac, VHT80 MCS9                                 | 0.41      | 0     | 82    | 108   | mA   |
| <b>5 GHz Wi-Fi 5 receive mode<sup>[3]</sup></b>      |           |       |       |       |      |
| 802.11a, 54 Mbit/s                                   | 0.41      | 0     | 54    | 118   | mA   |
| 802.11n, HT20 MCS7                                   | 0.41      | 0     | 55    | 120   | mA   |
| 802.11n, HT40 MCS7                                   | 0.41      | 0     | 65    | 140   | mA   |
| 802.11ac, VHT20 MCS8                                 | 0.41      | 0     | 55    | 120   | mA   |
| 802.11ac, VHT40 MCS9                                 | 0.41      | 0     | 65    | 140   | mA   |
| 802.11ac, VHT80 MCS9                                 | 0.41      | 0     | 70    | 158   | mA   |

Table 34. Current consumption...continued

| Mode                                                                         | VIO_3.3 V | 2.2 V | 1.8 V | 1.1 V | Unit |
|------------------------------------------------------------------------------|-----------|-------|-------|-------|------|
| <b>2.4 GHz Wi-Fi transmit mode</b> <sup>[3]</sup>                            |           |       |       |       |      |
| 802.11b, 11 Mbit/s at 20 dBm                                                 | 0.41      | 400   | 80    | 221   | mA   |
| 802.11g, 54 Mbit/s at 20 dBm                                                 | 0.41      | 377   | 79    | 220   | mA   |
| 802.11n, HT20 MCS0 at 20 dBm                                                 | 0.41      | 382   | 80    | 238   | mA   |
| 802.11n, HT20 MCS7 at 20 dBm                                                 | 0.41      | 382   | 80    | 238   | mA   |
| <b>5 GHz Wi-Fi transmit mode</b> <sup>[3]</sup>                              |           |       |       |       |      |
| 802.11a, 6 Mbit/s at 19 dBm                                                  | 0.41      | 285   | 141   | 215   | mA   |
| 802.11a, 54 Mbit/s at 19 dBm                                                 | 0.41      | 285   | 141   | 220   | mA   |
| 802.11n, HT20 MCS0 at 19 dBm                                                 | 0.41      | 290   | 145   | 238   | mA   |
| 802.11n, HT20 MCS7 at 19 dBm                                                 | 0.41      | 290   | 145   | 238   | mA   |
| 802.11n, HT40 MCS0 at 17 dBm                                                 | 0.41      | 230   | 138   | 239   | mA   |
| 802.11n, HT40 MCS7 at 17 dBm                                                 | 0.41      | 230   | 138   | 239   | mA   |
| 802.11ac, VHT20 MCS0 at 19 dBm                                               | 0.41      | 290   | 144   | 235   | mA   |
| 802.11ac, VHT20 MCS8 at 19 dBm                                               | 0.41      | 290   | 144   | 235   | mA   |
| 802.11ac, VHT40 MCS0 at 17 dBm                                               | 0.41      | 230   | 138   | 238   | mA   |
| 802.11ac, VHT40 MCS9 at 17 dBm                                               | 0.41      | 230   | 138   | 238   | mA   |
| 802.11ac, VHT80 MCS0 at 15 dBm                                               | 0.41      | 190   | 132   | 232   | mA   |
| 802.11ac, VHT80 MCS9 at 15 dBm                                               | 0.41      | 190   | 132   | 232   | mA   |
| <b>Peak current consumption during device initialization</b>                 |           |       |       |       |      |
| Maximum peak current consumption during device initialization <sup>[4]</sup> | 0.41      | 1040  | 223   | 231   | mA   |

[1] Wi-Fi core in sleep mode

[2] Beacon interval = 100 ms. Bluetooth not enabled

[3] Bluetooth in deep-sleep mode

[4] Ambient temperature 85°C

## 9.6 SDIO host interface specifications

The SDIO host interface pins are powered by VIO\_SD voltage supply.

The SDIO electrical specifications are identical for the 4-bit SDIO and 1-bit SDIO modes.

### 9.6.1 VIO\_SD DC characteristics

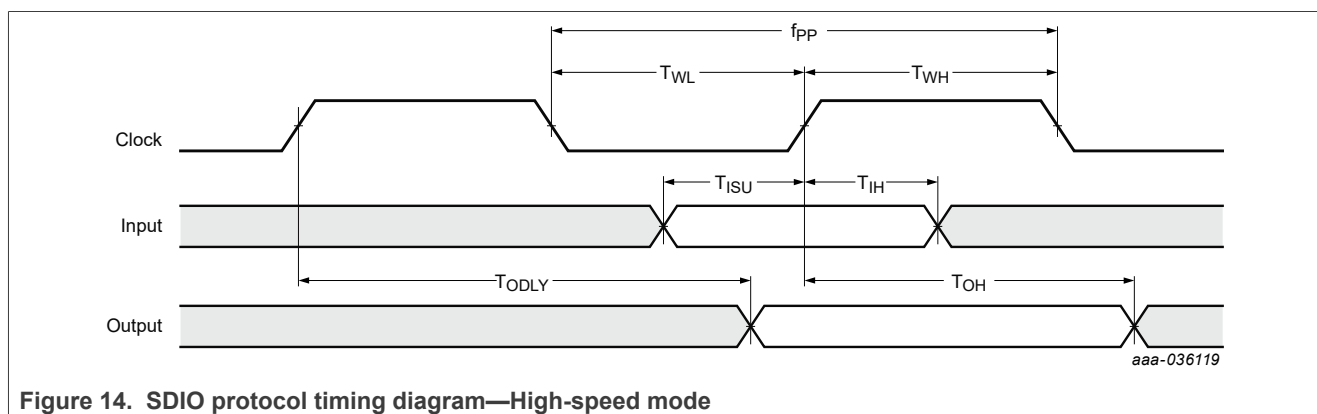
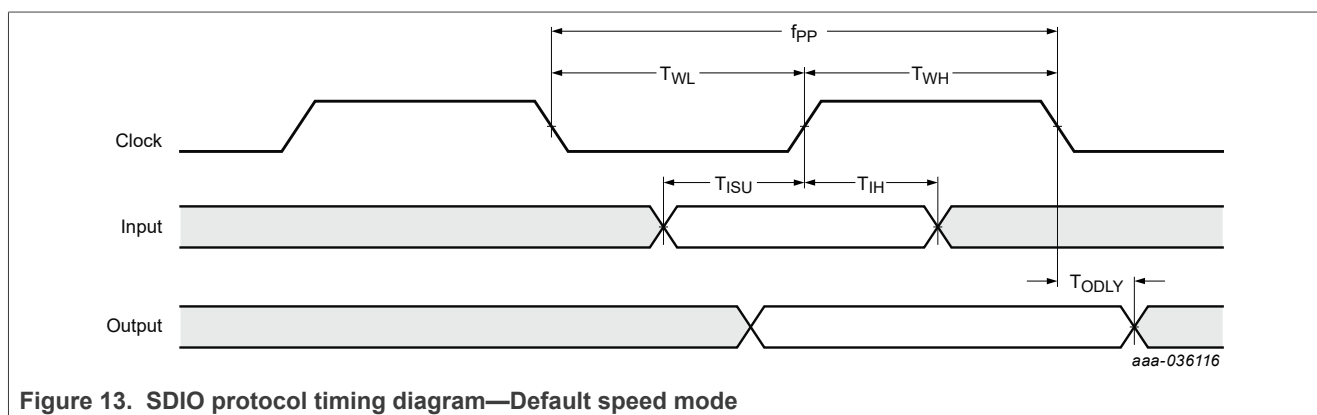
#### 9.6.1.1 1.8V operation

**Table 35. DC electrical characteristics—1.8V operation (VIO\_SD)**

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol           | Parameter           | Condition | Min        | Typ | Max        | Unit |
|------------------|---------------------|-----------|------------|-----|------------|------|
| V <sub>IH</sub>  | Input high voltage  | --        | 0.7*VIO_SD | --  | VIO_SD+0.4 | V    |
| V <sub>IL</sub>  | Input low voltage   | --        | -0.4       | --  | 0.3*VIO_SD | V    |
| V <sub>HYS</sub> | Input hysteresis    | --        | 100        | --  | --         | mV   |
| V <sub>OH</sub>  | Output high voltage | --        | VIO_SD-0.4 | --  | --         | V    |
| V <sub>OL</sub>  | Output low voltage  | --        | --         | --  | 0.4        | V    |

### 9.6.2 Default speed, high-speed modes



**Table 36. SDIO timing data—Default Speed, High-Speed Modes**

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol            | Parameter           | Condition  | Min | Typ | Max | Unit |
|-------------------|---------------------|------------|-----|-----|-----|------|
| f <sub>PP</sub>   | Clock frequency     | Normal     | 0   | --  | 25  | MHz  |
|                   |                     | High-speed | 0   | --  | 50  | MHz  |
| T <sub>WL</sub>   | Clock low time      | Normal     | 10  | --  | --  | ns   |
|                   |                     | High-speed | 7   | --  | --  | ns   |
| T <sub>WH</sub>   | Clock high time     | Normal     | 10  | --  | --  | ns   |
|                   |                     | High-speed | 7   | --  | --  | ns   |
| T <sub>ISU</sub>  | Input setup time    | Normal     | 5   | --  | --  | ns   |
|                   |                     | High-speed | 6   | --  | --  | ns   |
| T <sub>IH</sub>   | Input hold time     | Normal     | 5   | --  | --  | ns   |
|                   |                     | High-speed | 2   | --  | --  | ns   |
| T <sub>ODLY</sub> | Output delay time   | Normal     | --  | --  | 14  | ns   |
|                   | CL ≤ 40 pF (1 card) | High-speed | --  | --  | 14  | ns   |
| T <sub>OH</sub>   | Output hold time    | High-speed | 2.5 | --  | --  | ns   |

## 9.6.3 SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

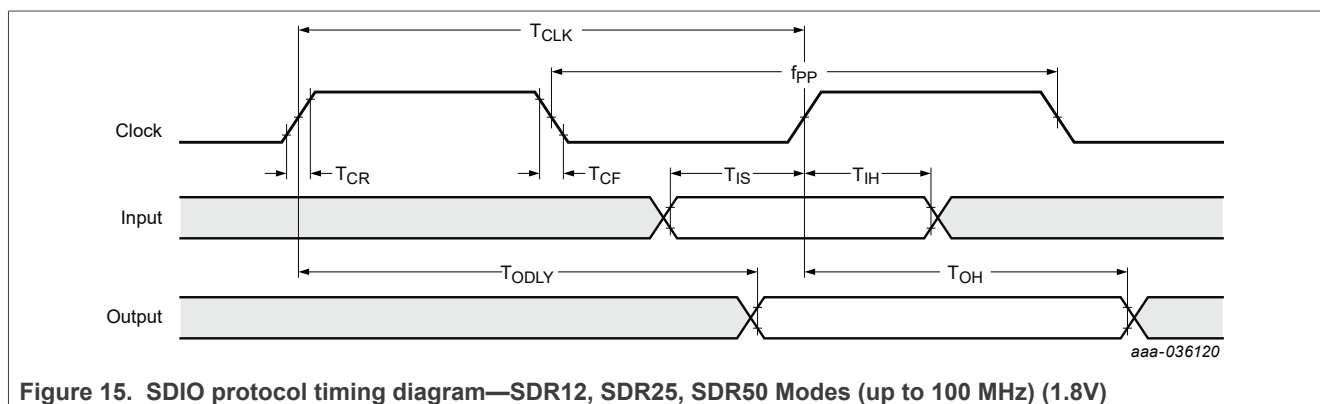


Table 37. SDIO timing data—SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8V)

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol           | Parameter                                                                                 | Condition   | Min | Typ | Max                 | Units |
|------------------|-------------------------------------------------------------------------------------------|-------------|-----|-----|---------------------|-------|
| $f_{PP}$         | Clock frequency                                                                           | SDR12/25/50 | 25  | --  | 100                 | MHz   |
| $T_{IS}$         | Input setup time                                                                          | SDR12/25/50 | 3   | --  | --                  | ns    |
| $T_{IH}$         | Input hold time                                                                           | SDR12/25/50 | 0.8 | --  | --                  | ns    |
| $T_{CLK}$        | Clock time                                                                                | SDR12/25/50 | 10  | --  | 40                  | ns    |
| $T_{CR}, T_{CF}$ | Rise time, fall time<br>$T_{CR}, T_{CF} < 2$ ns (max) at<br>100 MHz<br>$C_{CARD} = 10$ pF | SDR12/25/50 | --  | --  | $0.2 \cdot T_{CLK}$ | ns    |
| $T_{ODLY}$       | Output delay time<br>$C_L \leq 30$ pF                                                     | SDR12/25/50 | --  | --  | 7.5                 | ns    |
| $T_{OH}$         | Output hold time<br>$C_L = 15$ pF                                                         | SDR12/25/50 | 1.5 | --  | --                  | ns    |

## 9.6.4 SDR104 mode (208 MHz) (1.8V)

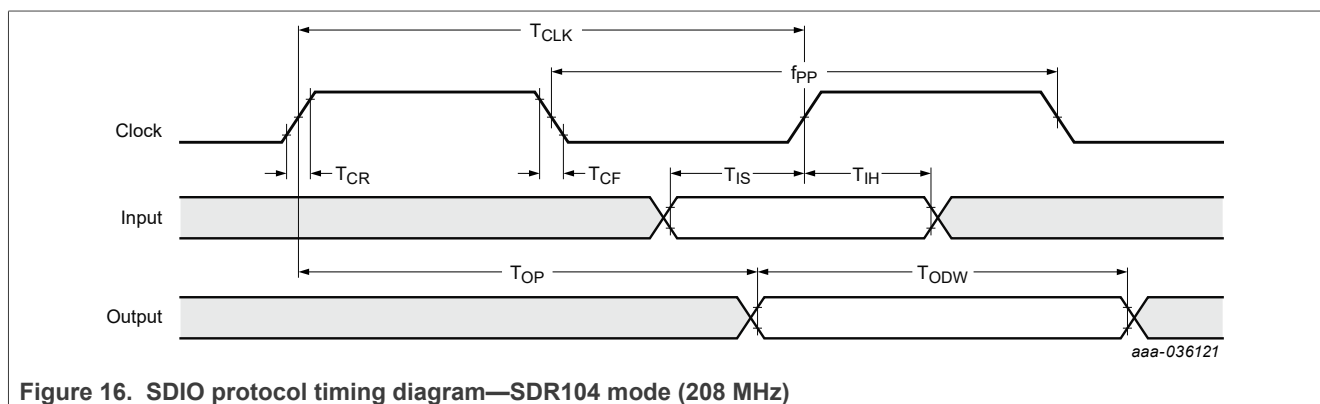


Table 38. SDIO timing data—SDR104 mode (208 MHz)

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol           | Parameter                                                                                 | Condition | Min  | Typ | Max                 | Unit |
|------------------|-------------------------------------------------------------------------------------------|-----------|------|-----|---------------------|------|
| $f_{PP}$         | Clock frequency                                                                           | SDR104    | 0    | --  | 208                 | MHz  |
| $T_{IS}$         | Input setup time                                                                          | SDR104    | 1.4  | --  | --                  | ns   |
| $T_{IH}$         | Input hold time                                                                           | SDR104    | 0.8  | --  | --                  | ns   |
| $T_{CLK}$        | Clock time                                                                                | SDR104    | 4.8  | --  | --                  | ns   |
| $T_{CR}, T_{CF}$ | Rise time, fall time<br>$T_{CR}, T_{CF} < 0.96$ ns (max) at 208 MHz<br>$C_{CARD} = 10$ pF | SDR104    | --   | --  | $0.2 \cdot T_{CLK}$ | ns   |
| $T_{OP}$         | Card output phase                                                                         | SDR104    | 0    | --  | 10                  | ns   |
| $T_{ODW}$        | Output timing of variable data window                                                     | SDR104    | 2.88 | --  | --                  | ns   |

## 9.6.5 DDR50 mode (50 MHz) (1.8V)

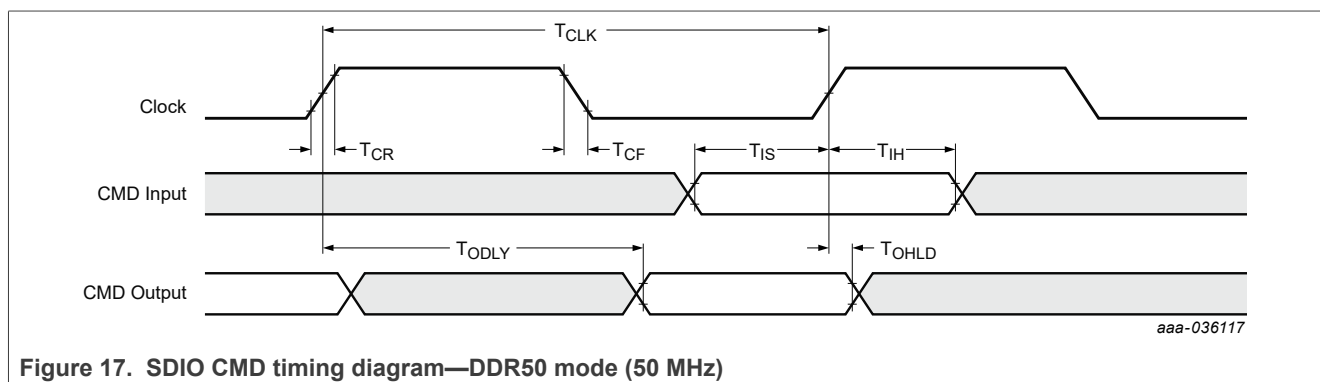
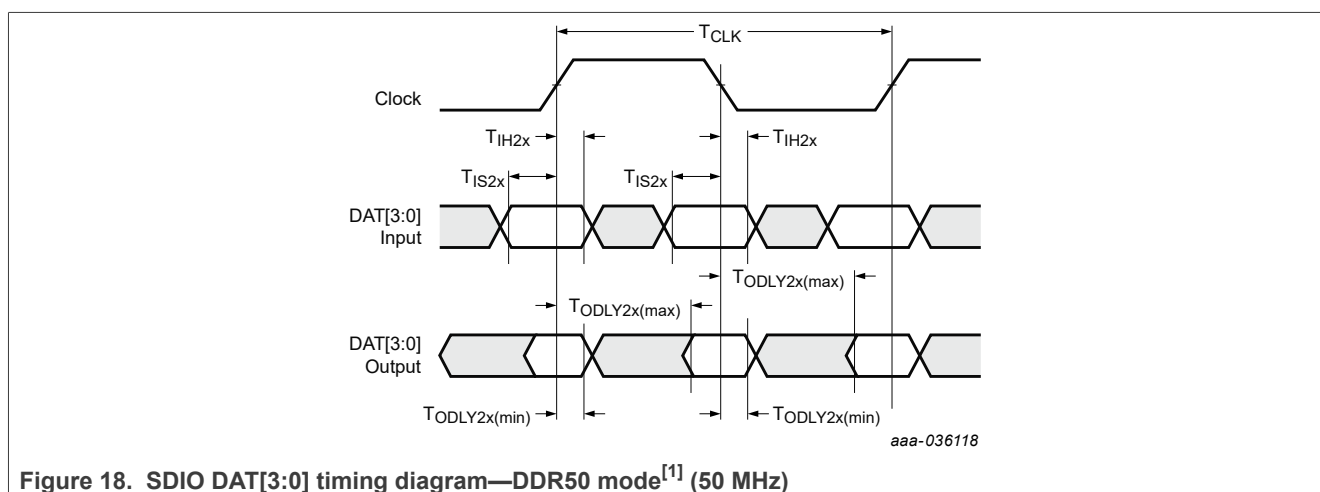


Figure 17. SDIO CMD timing diagram—DDR50 mode (50 MHz)

Figure 18. SDIO DAT[3:0] timing diagram—DDR50 mode<sup>[1]</sup> (50 MHz)

[1] In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

Table 39. SDIO timing data—DDR50 mode (50 MHz)

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol                                             | Parameter                                                                                   | Condition | Min | Typ | Max                 | Units |
|----------------------------------------------------|---------------------------------------------------------------------------------------------|-----------|-----|-----|---------------------|-------|
| <b>Clock</b>                                       |                                                                                             |           |     |     |                     |       |
| $T_{CLK}$                                          | Clock time<br>50 MHz (max) between<br>rising edges                                          | DDR50     | 20  | --  | --                  | ns    |
| $T_{CR}, T_{CF}$                                   | Rise time, fall time<br>$T_{CR}, T_{CF} < 4.00$ ns (max) at<br>50 MHz<br>$C_{CARD} = 10$ pF | DDR50     | --  | --  | $0.2 \cdot T_{CLK}$ | ns    |
| Clock Duty                                         | --                                                                                          | DDR50     | 45  | --  | 55                  | %     |
| <b>CMD Input (referenced to clock rising edge)</b> |                                                                                             |           |     |     |                     |       |
| $T_{IS}$                                           | Input setup time<br>$C_{CARD} \leq 10$ pF (1 card)                                          | DDR50     | 6   | --  | --                  | ns    |

Table 39. SDIO timing data—DDR50 mode (50 MHz)...continued

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol                                                                | Parameter                                                                | Condition | Min | Typ | Max  | Units |
|-----------------------------------------------------------------------|--------------------------------------------------------------------------|-----------|-----|-----|------|-------|
| $T_{IH}$                                                              | Input hold time<br>$C_{CARD} \leq 10$ pF (1 card)                        | DDR50     | 0.8 | --  | --   | ns    |
| <b>CMD Output (referenced to clock rising edge)</b>                   |                                                                          |           |     |     |      |       |
| $T_{ODLY}$                                                            | Output delay time during data transfer mode<br>$C_L \leq 30$ pF (1 card) | DDR50     | --  | --  | 13.7 | ns    |
| $T_{OHL D}$                                                           | Output hold time<br>$C_L \geq 15$ pF (1 card)                            | DDR50     | 1.5 | --  | --   | ns    |
| <b>DAT[3:0] Input (referenced to clock rising and falling edges)</b>  |                                                                          |           |     |     |      |       |
| $T_{IS2x}$                                                            | Input setup time<br>$C_{CARD} \leq 10$ pF (1 card)                       | DDR50     | 3   | --  | --   | ns    |
| $T_{IH2x}$                                                            | Input hold time<br>$C_{CARD} \leq 10$ pF (1 card)                        | DDR50     | 0.8 | --  | --   | ns    |
| <b>DAT[3:0] Output (referenced to clock rising and falling edges)</b> |                                                                          |           |     |     |      |       |
| $T_{ODLY2x (max)}$                                                    | Output delay time during data transfer mode<br>$C_L \leq 25$ pF (1 card) | DDR50     | --  | --  | 7.0  | ns    |
| $T_{ODLY2x (min)}$                                                    | Output hold time<br>$C_L \geq 15$ pF (1 card)                            | DDR50     | 1.5 | --  | --   | ns    |

### 9.6.6 SDIO internal pull-up/pull-down specifications

Table 40. SDIO internal pull-up/pull-down specifications

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Parameter                                     | Condition | Min | Typ | Max | Unit       |
|-----------------------------------------------|-----------|-----|-----|-----|------------|
| Internal nominal pull-up/pull-down resistance | --        | 60  | 90  | 120 | k $\Omega$ |

9.7 High-speed UART specifications

The UART Tx and Rx pins are powered by VIO voltage supply.  
See [Section 9.1.1 "VIO DC characteristics"](#) for DC specifications.

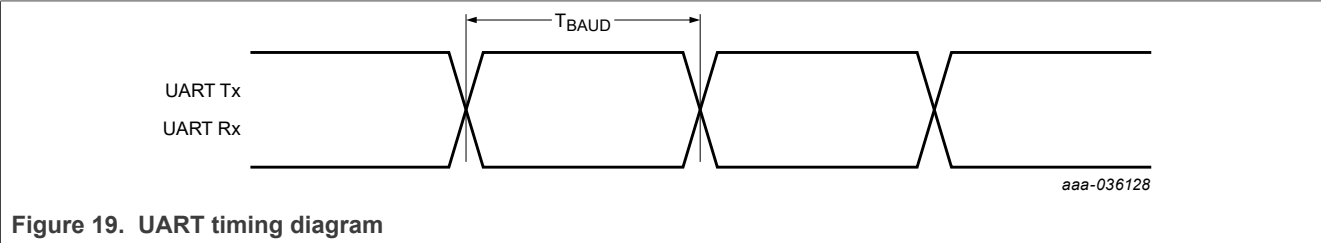


Table 41. UART timing data<sup>[1]</sup>  
Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol            | Parameter | Condition            | Min | Typ | Max | Unit |
|-------------------|-----------|----------------------|-----|-----|-----|------|
| T <sub>BAUD</sub> | Baud rate | 38.4 MHz input clock | 250 | --  | --  | ns   |

[1] The acceptable deviation from the UART Rx target baud rate is ±3%.

9.8 Audio interface specifications

9.8.1 PCM interface specifications

The PCM pins are powered by VIO voltage supply. See [Section 9.1.1 "VIO DC characteristics"](#) for specifications.

## Central Mode

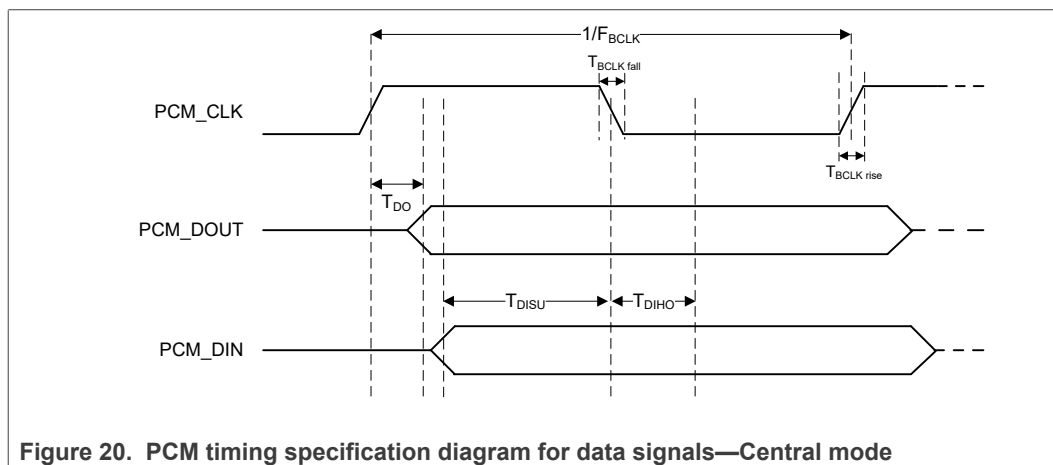


Figure 20. PCM timing specification diagram for data signals—Central mode

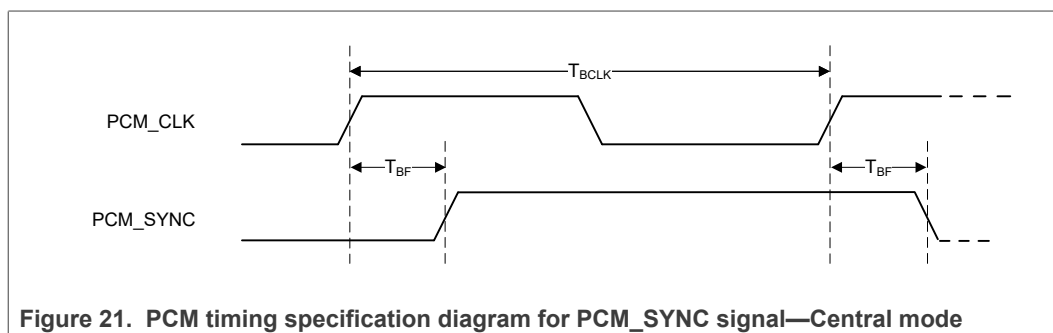


Figure 21. PCM timing specification diagram for PCM\_SYNC signal—Central mode

Table 42. PCM timing specification data—Central mode

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol                       | Parameter                                              | Condition | Min | Typ     | Max   | Unit |
|------------------------------|--------------------------------------------------------|-----------|-----|---------|-------|------|
| $F_{BCLK}$                   | Bit clock frequency                                    | --        | 2   | 2/2.048 | 2.048 | MHz  |
| Duty Cycle <sub>BCLK</sub>   | Bit clock duty cycle                                   | --        | 0.4 | 0.5     | 0.6   | --   |
| $T_{BCLK \text{ rise/fall}}$ | PCM_CLK rise/fall time                                 | --        | --  | 3       | --    | ns   |
| $T_{DO}$                     | Delay from PCM_CLK rising edge to PCM_DOUT rising edge | --        | --  | --      | 15    | ns   |
| $T_{DISU}$                   | Setup time for PCM_DIN before PCM_CLK falling edge     | --        | 20  | --      | --    | ns   |
| $T_{DIHO}$                   | Hold time for PCM_DIN after PCM_CLK falling edge       | --        | 15  | --      | --    | ns   |
| $T_{BF}$                     | Delay from PCM_CLK rising edge to PCM_SYNC rising edge | --        | --  | --      | 15    | ns   |

## Peripheral mode

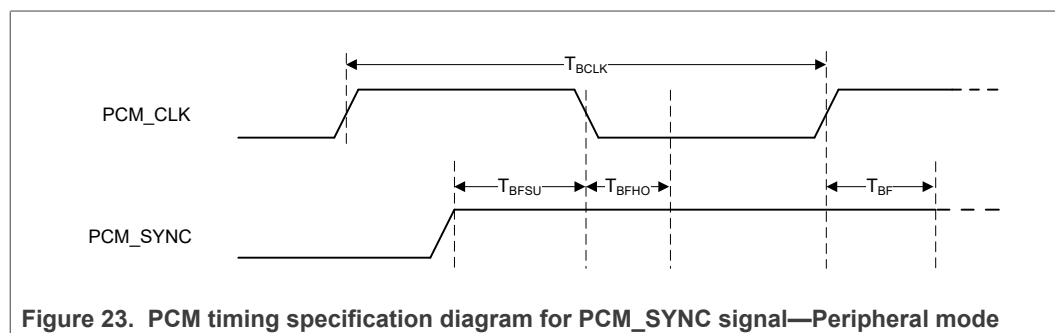
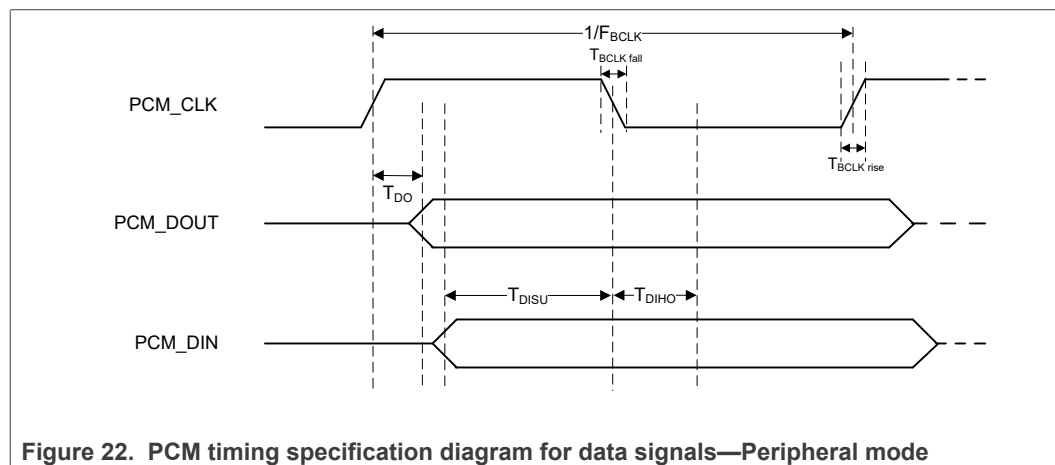


Table 43. PCM timing specification data—Peripheral mode

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol                       | Parameter                                              | Condition | Min   | Typ     | Max | Unit |
|------------------------------|--------------------------------------------------------|-----------|-------|---------|-----|------|
| $F_{BCLK}$                   | Bit clock frequency                                    | --        | 0.512 | 2/2.048 | 4   | MHz  |
| Duty Cycle <sub>BCLK</sub>   | Bit clock duty cycle                                   | --        | 0.4   | 0.5     | 0.6 | --   |
| $T_{BCLK \text{ rise/fall}}$ | PCM_CLK rise/fall time                                 | --        | --    | 3       | --  | ns   |
| $T_{DO}$                     | Delay from PCM_CLK rising edge to PCM_DOUT rising edge | --        | --    | --      | 30  | ns   |
| $T_{DISU}$                   | Setup time for PCM_DIN before PCM_CLK falling edge     | --        | 15    | --      | --  | ns   |
| $T_{DIHO}$                   | Hold time for PCM_DIN after PCM_CLK falling edge       | --        | 10    | --      | --  | ns   |
| $T_{BFSU}$                   | Setup time for PCM_SYNC before PCM_CLK falling edge    | --        | 15    | --      | --  | ns   |
| $T_{BFHO}$                   | Hold time for PCM_SYNC after PCM_CLK falling edge      | --        | 10    | --      | --  | ns   |

## 9.9 Reference clock specifications

### 9.9.1 External crystal oscillator specifications

The reference clock from the external crystal oscillator requires a CMOS input signal.

**Note:** All new designs should use the 38.4 MHz reference clock. For existing designs the 26 MHz reference clock can still be used.

Table 44. Clock DC specifications<sup>[1]</sup>

| Parameter                       | Condition | Min | Typ | Max | Unit |
|---------------------------------|-----------|-----|-----|-----|------|
| Single-ended high-level voltage | --        | --  | --  | 1.8 | V    |
| Single-ended low-level voltage  | --        | 0   | --  | --  | V    |
| Clock amplitude (pk-pk)         | --        | 0.5 | --  | 1   | V    |
| Mid-point slope                 | --        | 125 | --  | --  | MV/s |

[1] The AC-coupling capacitor is integrated into the SoC.

Table 45. 26 MHz clock timing

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Parameter       | Condition | Min            | Typ   | Max            | Unit |
|-----------------|-----------|----------------|-------|----------------|------|
| XO26 period     | --        | 38.46 - 20 ppm | 38.46 | 38.46 + 20 ppm | ns   |
| XO26 rise time  | --        | --             | --    | 5.00           | ns   |
| XO26 fall time  | --        | --             | --    | 5.00           | ns   |
| XO26 duty cycle | --        | 48.05          | 50    | 51.95          | %    |

Table 46. 38.4 MHz clock timing

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Parameter         | Condition | Min            | Typ   | Max            | Unit |
|-------------------|-----------|----------------|-------|----------------|------|
| XO38_4 period     | --        | 26.04 - 20 ppm | 26.04 | 26.04 + 20 ppm | ns   |
| XO38_4 rise time  | --        | --             | --    | 2.50           | ns   |
| XO38_4 fall time  | --        | --             | --    | 2.50           | ns   |
| XO38_4 duty cycle | --        | 47.12          | 50    | 52.88          | %    |

Table 47. Phase Noise—2.4 GHz operation

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Parameter       | Test Conditions  | Min | Typ | Max  | Unit   |
|-----------------|------------------|-----|-----|------|--------|
| Fref = 26 MHz   | Offset = 1 kHz   | --  | --  | -126 | dBc/Hz |
|                 | Offset = 10 kHz  | --  | --  | -137 | dBc/Hz |
|                 | Offset = 100 kHz | --  | --  | -145 | dBc/Hz |
|                 | Offset > 1 MHz   | --  | --  | -145 | dBc/Hz |
| Fref = 38.4 MHz | Offset = 1 kHz   | --  | --  | -123 | dBc/Hz |
|                 | Offset = 10 kHz  | --  | --  | -134 | dBc/Hz |
|                 | Offset = 100 kHz | --  | --  | -142 | dBc/Hz |
|                 | Offset > 1 MHz   | --  | --  | -142 | dBc/Hz |

Table 48. Phase Noise—5 GHz operation

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Parameter       | Test Conditions  | Min | Typ | Max  | Unit   |
|-----------------|------------------|-----|-----|------|--------|
| Fref = 26 MHz   | Offset = 1 kHz   | --  | --  | -130 | dBc/Hz |
|                 | Offset = 10 kHz  | --  | --  | -150 | dBc/Hz |
|                 | Offset = 100 kHz | --  | --  | -156 | dBc/Hz |
|                 | Offset > 1 MHz   | --  | --  | -156 | dBc/Hz |
| Fref = 38.4 MHz | Offset = 1 kHz   | --  | --  | -126 | dBc/Hz |
|                 | Offset = 10 kHz  | --  | --  | -146 | dBc/Hz |
|                 | Offset = 100 kHz | --  | --  | -154 | dBc/Hz |
|                 | Offset > 1 MHz   | --  | --  | -154 | dBc/Hz |

### 9.9.2 External crystal specifications

**Note:** All new designs should use the 38.4 MHz reference clock. For existing designs the 26 MHz reference clock can still be used.

Table 49. External crystal specifications

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Parameter                                | Condition                  | Min | Typ                | Max | Unit            |
|------------------------------------------|----------------------------|-----|--------------------|-----|-----------------|
| Fundamental frequencies                  | --                         | --  | 26 or 38.4         | --  | MHz             |
| Resonance mode                           | --                         | --  | A1,<br>Fundamental | --  | --              |
| Equivalent differential load capacitance | --                         | --  | 5                  | --  | pF              |
| Shunt capacitance                        | --                         | --  | 2                  | --  | pF              |
| Frequency tolerance                      | Over process at 25°C       | --  | ±10                | --  | ppm             |
| Frequency stability                      | Over operating temperature | --  | ±10                | --  | ppm             |
| Aging                                    | --                         | --  | ±2                 | --  | ppm/<br>5 years |
| Series resistance (ESR)                  | 38.4 MHz                   | --  | --                 | 60  | Ω               |
|                                          | 26 MHz                     | --  | --                 | 60  | Ω               |
| Insulation resistance                    | at DC 100V                 | 500 | --                 | --  | MΩ              |
| Drive level                              | --                         | 150 | --                 | --  | μW              |

### 9.9.3 External sleep clock specifications

Table 50. External sleep clock specifications<sup>[1]</sup>

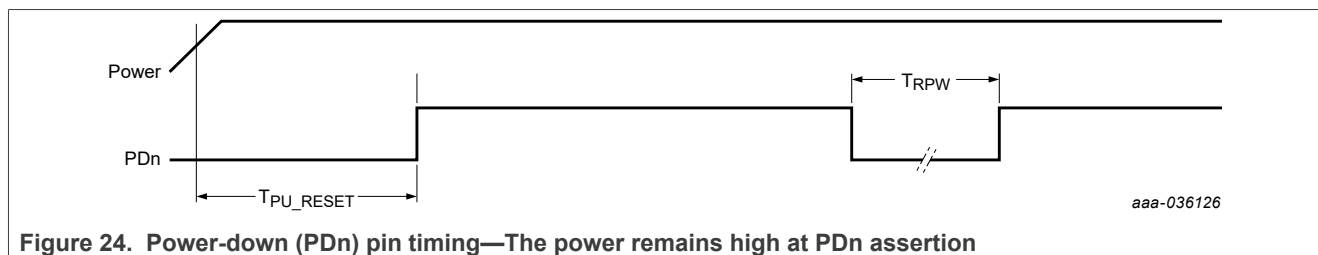
| Parameter                                | Min | Typ    | Max | Units    |
|------------------------------------------|-----|--------|-----|----------|
| Clock frequency range/accuracy           | --  | 32.768 | --  | kHz      |
| • CMOS input clock signal type           |     |        |     |          |
| • ±250 ppm (initial, aging, temperature) |     |        |     |          |
| Phase noise requirement (@ 100 kHz)      | --  | -125   | --  | dBc/Hz   |
| Cycle jitter                             | --  | 1.5    | --  | ns (RMS) |
| Slew rate limit (10-90%)                 | --  | --     | 100 | ns       |
| Duty cycle tolerance                     | 20  | --     | 80  | %        |

[1] Voltage input levels = 1.8V or 3.3V. See [Section 8 "Recommended operating conditions"](#).

## 9.10 Power-down (PDn) pin specifications

### 9.10.1 PDn asserted low—All power supplies good

Figure 24 and Table 51 show the specifications for the PDn signal when it is asserted (low) while all power supplies to the device are good.



**Table 51. Power-down (PDn) pin specifications—The power remains high at PDn assertion**

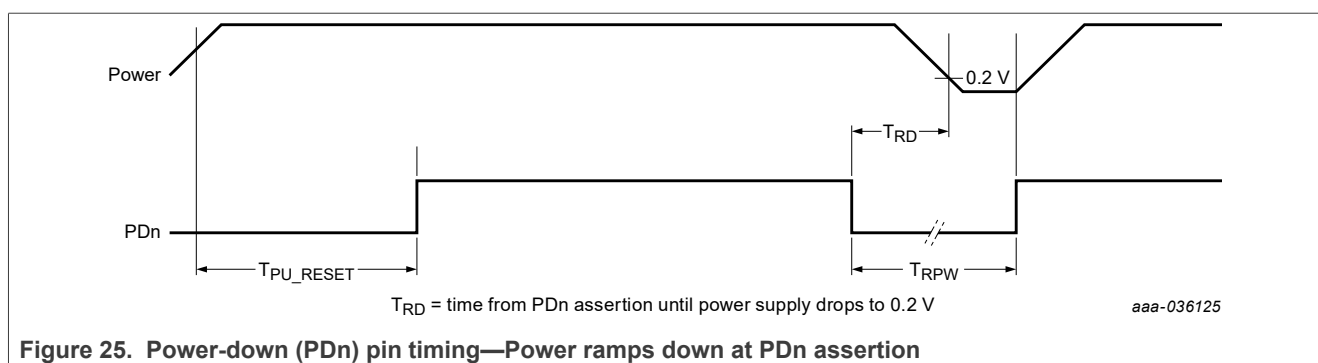
Unless otherwise specified, the values apply per the Recommended operating conditions

| Symbol          | Parameter                      | Condition | Min              | Typ | Max | Unit |
|-----------------|--------------------------------|-----------|------------------|-----|-----|------|
| $T_{PU\_RESET}$ | Valid power to PDn de-asserted | --        | 0                | --  | --  | ms   |
| $T_{RPW}$       | PDn pulse width                | --        | 1 <sup>[1]</sup> | --  | --  | μs   |
| $V_{IH}$        | Input high voltage             | --        | 1.4              | --  | 4.5 | V    |
| $V_{IL}$        | Input low voltage              | --        | -0.4             | --  | 0.5 | V    |

[1] Minimum value guaranteed for a valid reset. Smaller values may put the device in an undefined state.

### 9.10.2 PDn asserted Low—One or more power supplies ramp down

Figure 25 and Table 52 show the specifications for the PDn signal when it is asserted (low) while 1 or more of the power supplies (including V<sub>CORE</sub>) ramps down.



**Table 52. Power-down (PDn) pin specifications—Power ramps down at PDn assertion**

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol                | Parameter                      | Condition | Min                            | Typ | Max | Unit |
|-----------------------|--------------------------------|-----------|--------------------------------|-----|-----|------|
| T <sub>PU_RESET</sub> | Valid power to PDn de-asserted | --        | 0                              | —   | —   | ms   |
| T <sub>RPW</sub>      | PDn pulse width                | --        | T <sub>RD</sub> <sup>[1]</sup> | —   | —   | μs   |
| V <sub>IH</sub>       | Input high voltage             | --        | 1.4                            | —   | 4.5 | V    |
| V <sub>IL</sub>       | Input low voltage              | --        | -0.4                           | —   | 0.2 | V    |

[1] Minimum value guaranteed for a valid reset. Smaller values may put the device in an undefined state.

## 9.11 Configuration pin specifications

For a list of configuration pins, see [Section 5.6 "Configuration pins"](#).

**Table 53. Configuration pin specifications<sup>[1]</sup>**

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Parameter                           | Condition                       | Min | Typ | Max | Unit |
|-------------------------------------|---------------------------------|-----|-----|-----|------|
| Internal weak pull-up resistance    | Around 1 ms following any reset | —   | 800 | —   | kΩ   |
| Internal nominal pull-up resistance | Around 1 ms following any reset | —   | 100 | —   | kΩ   |

[1] After approximately 1 ms, the configuration pins become functional pins.

## 9.12 JTAG interface specifications

The test interface pins are powered by VIO voltage supply.

See [Section 9.1.1 "VIO DC characteristics"](#) for specifications.

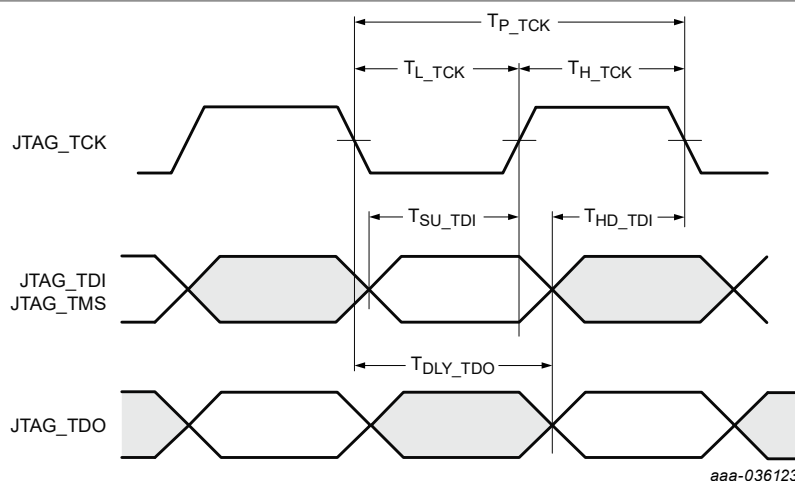


Figure 26. JTAG timing diagram

Table 54. JTAG timing data<sup>[1]</sup>

Unless otherwise specified, the values apply per [Section 8 "Recommended operating conditions"](#)

| Symbol         | Parameter                  | Condition | Min | Typ | Max | Unit |
|----------------|----------------------------|-----------|-----|-----|-----|------|
| $T_{P\_TCK}$   | TCK period                 | --        | 40  | --  | --  | ns   |
| $T_{H\_TCK}$   | TCK high                   | --        | 12  | --  | --  | ns   |
| $T_{L\_TCK}$   | TCK low                    | --        | 12  | --  | --  | ns   |
| $T_{SU\_TDI}$  | TDI, TMS to TCK setup time | --        | 10  | --  | --  | ns   |
| $T_{HD\_TDI}$  | TDI, TMS to TCK hold time  | --        | 10  | --  | --  | ns   |
| $T_{DLY\_TDO}$ | TCK to TDO delay           | --        | 0   | --  | 15  | ns   |

[1] Does not apply to JTAG enabled by the JTAG\_TMS pin.

## 10 Package information

### 10.1 Package thermal conditions

#### 10.1.1 68-pin QFN thermal conditions

Table 55. Thermal conditions—QFN package

| Symbol        | Parameter                                                                                                                                                                                            | Condition                                                | Typ   | Unit |
|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|-------|------|
| $\theta_{JA}$ | Thermal resistance<br>Junction to ambient of package.<br>$\theta_{JA} = (T_J - T_A) / P$<br>$P$ = total power dissipation                                                                            | 24 x 30 x 1.05 mm<br>6-layer PCB<br>no air flow          | 43.00 | °C/W |
|               |                                                                                                                                                                                                      | 24 x 30 x 1.05 mm<br>6-layer PCB<br>1 meter/sec air flow | 36.90 | °C/W |
|               |                                                                                                                                                                                                      | 24 x 30 x 1.05 mm<br>6-layer PCB<br>2 meter/sec air flow | 32.50 | °C/W |
|               |                                                                                                                                                                                                      | 24 x 30 x 1.05 mm<br>6-layer PCB<br>3 meter/sec air flow | 30.30 | °C/W |
| $\psi_{JT}$   | Thermal characteristic parameter<br>Junction to top-center of package.<br>$\psi_{JT} = (T_J - T_{TOP}) / P$<br>$T_{TOP}$ = temperature on top-center of package                                      | 24 x 30 x 1.05 mm<br>6-layer PCB<br>no air flow          | 4.10  | °C/W |
| $\psi_{JB}$   | Thermal characteristic parameter<br>Junction to bottom surface, center of package.<br>$\psi_{JB} = (T_J - T_B) / P$<br>$T_B$ = surface temperature of package                                        | 24 x 30 x 1.05 mm<br>6-layer PCB<br>no air flow          | 13.80 | °C/W |
| $\theta_{JC}$ | Thermal resistance<br>Junction to case of the package.<br>$\theta_{JC} = (T_J - T_C) / P_{TOP}$<br>$T_C$ = temperature on top-center of package<br>$P_{TOP}$ = power dissipation from top of package | 24 x 30 x 1.05 mm<br>6-layer PCB<br>no air flow          | 13.80 | °C/W |
| $\theta_{JB}$ | Thermal resistance<br>Junction to board of package.<br>$\theta_{JB} = (T_J - T_B) / P_{BOTTOM}$<br>$P_{BOTTOM}$ = power dissipation from bottom of package to PCB surface                            | 24 x 30 x 1.05 mm<br>6-layer PCB<br>no air flow          | 14.10 | °C/W |

## 10.1.2 83-bump eWLP thermal conditions

Table 56. Thermal conditions—eWLP package

| Symbol        | Parameter                                                                                                                                                       | Condition                                                               | Typ   | Unit |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|-------|------|
| $\theta_{JA}$ | Thermal resistance<br>Junction to ambient of package.<br>$\theta_{JA} = (T_J - T_A) / P$<br>P = total power dissipation                                         | JEDEC 4 in. x 4.5 in.<br>4-layer PCB with 41 thermal via<br>no air flow | 28.07 | °C/W |
|               |                                                                                                                                                                 | JEDEC 4 in. x 4.5 in.<br>4-layer PCB with no thermal via<br>no air flow | 41.96 | °C/W |
| $\psi_{JT}$   | Thermal characteristic parameter<br>Junction to top-center of package.<br>$\psi_{JT} = (T_J - T_{TOP}) / P$<br>$T_{TOP}$ = temperature on top-center of package | JEDEC 4 in. x 4.5 in.<br>4-layer PCB with no thermal via<br>no air flow | 0.08  | °C/W |
| $\psi_{JB}$   | Thermal characteristic parameter<br>Junction to bottom surface, center of package.<br>$\psi_{JB} = (T_J - T_B) / P$<br>$T_B$ = surface temperature of package   | JEDEC 4 in. x 4.5 in.<br>4-layer PCB with no thermal via<br>no air flow | 15.30 | °C/W |

10.2 Package mechanical drawing

10.2.1 68-pin QFN mechanical drawing

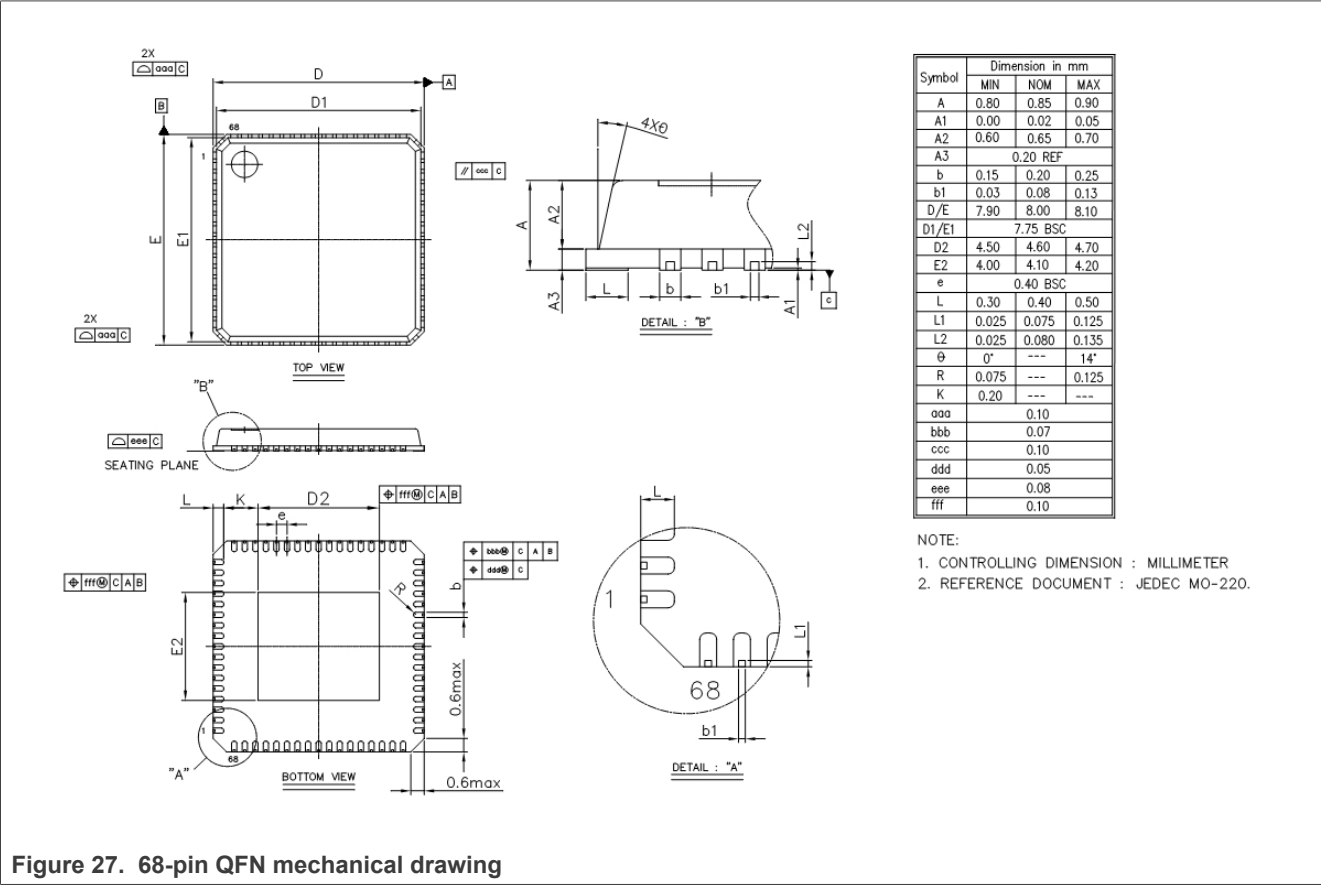


Figure 27. 68-pin QFN mechanical drawing

**Note:** See also [Section 10.1.1 "68-pin QFN thermal conditions"](#) and [Section 10.3.1 "68-pin QFN package marking"](#).

10.2.2 83-bump eWLP mechanical drawing

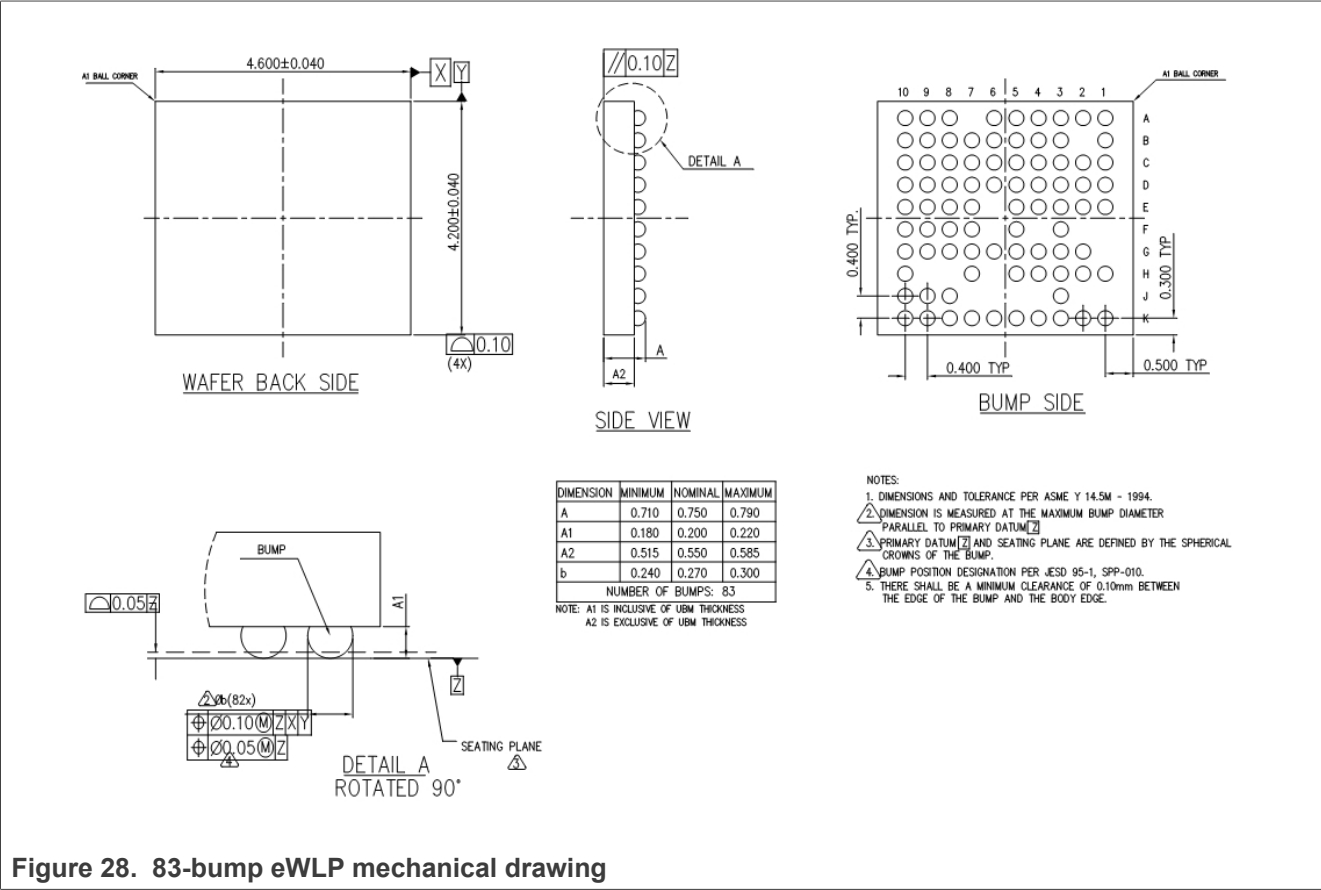
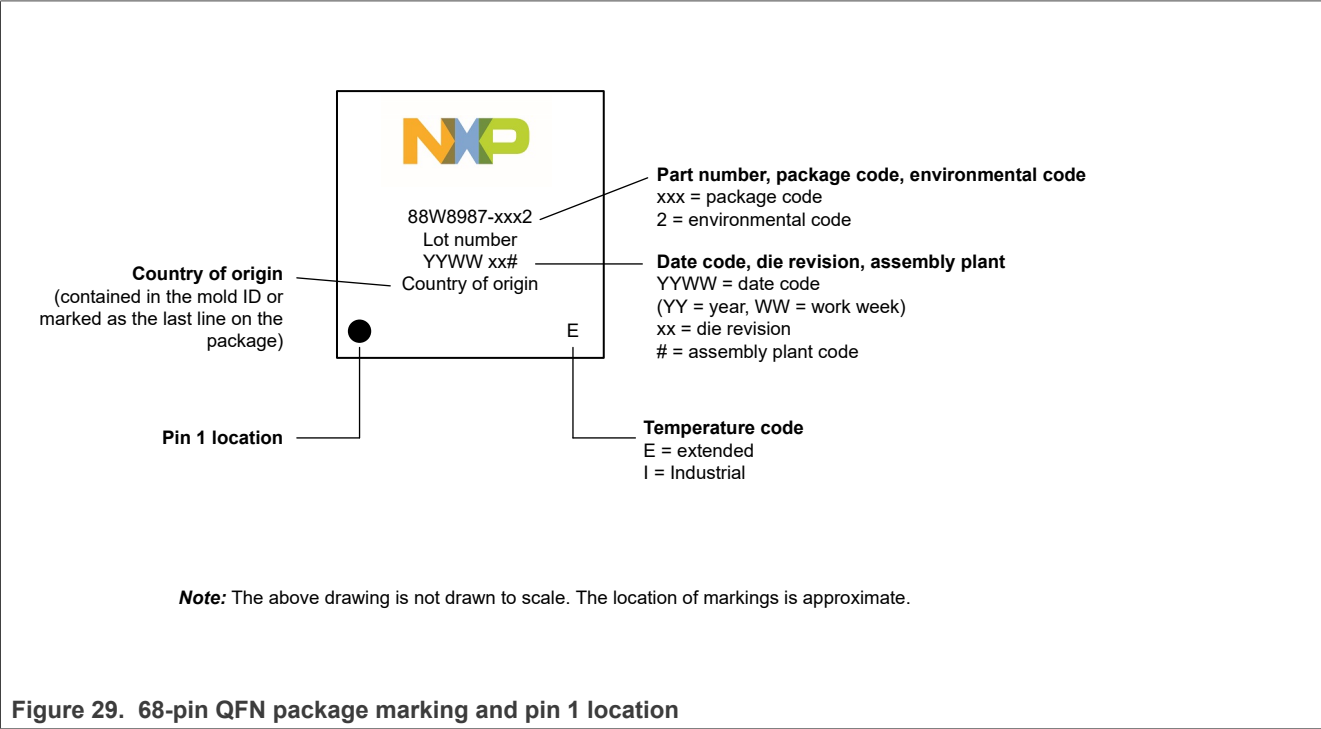


Figure 28. 83-bump eWLP mechanical drawing

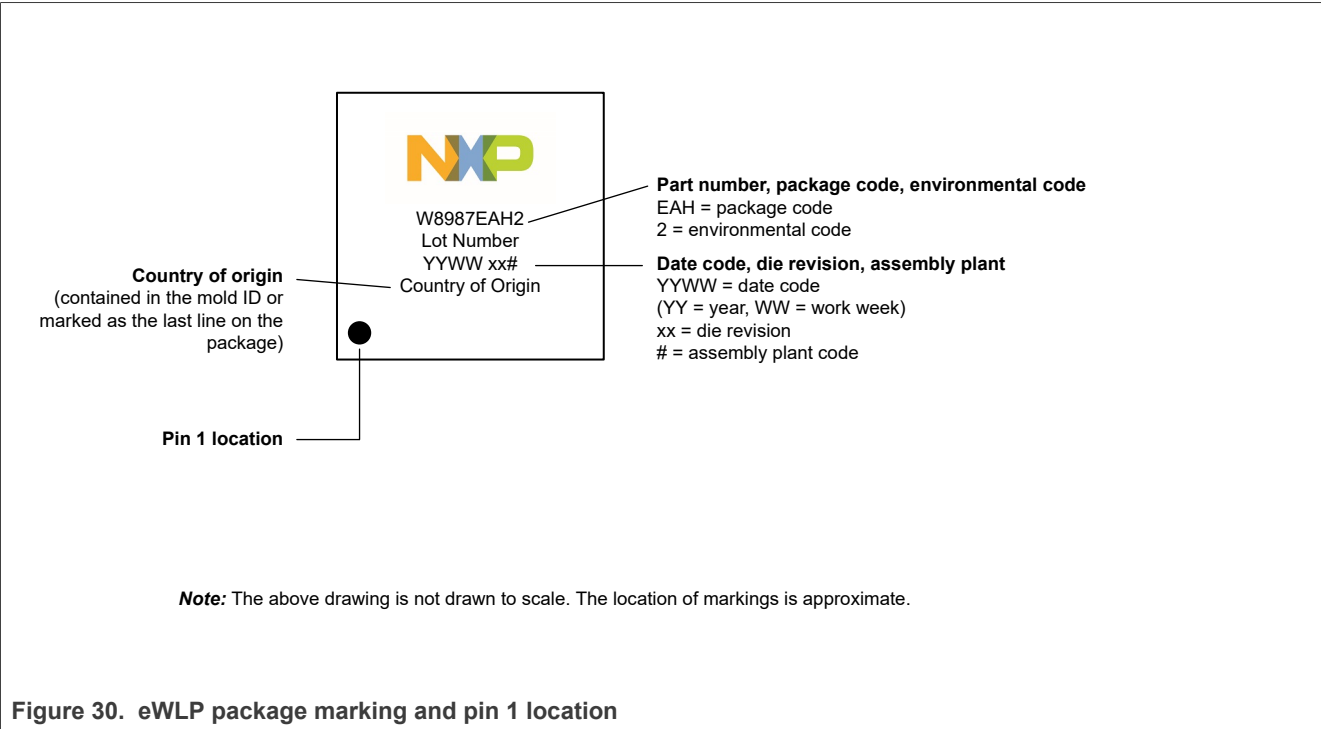
- Dimensions in mm. Also refer to [Section 10.1.2 "83-bump eWLP thermal conditions"](#) and [Section 10.3.2 "83-bump eWLP package marking"](#).

10.3 Package marking

10.3.1 68-pin QFN package marking



10.3.2 83-bump eWLP package marking



## 11 Acronyms and abbreviations

Table 57. Acronyms and abbreviations

| Acronym | Definition                                |
|---------|-------------------------------------------|
| A2DP    | Advanced audio distribution profiles      |
| ABR     | Automatic baud rate                       |
| ACK     | Acknowledgment                            |
| ADAS    | Advanced driver assistance systems        |
| ADC     | Analog-to-digital converter               |
| AES     | Advanced encryption standard              |
| AFC     | Automatic frequency correction            |
| AFH     | Adaptive frequency hopping                |
| AGC     | Automatic gain control                    |
| AHB     | Advanced high-performance bus             |
| AIFS    | Arbitration inter-frame space             |
| AoA     | Angle of arrival                          |
| AoD     | Angle of departure                        |
| AP      | Access point                              |
| APB     | Advanced peripheral bus                   |
| API     | Application program interface             |
| ARM     | Advanced RISC machine                     |
| ATIM    | Announcement traffic indication message   |
| BAMR    | Base address mask register                |
| BAR     | Base address register                     |
| BBU     | Baseband processor unit                   |
| BCB     | Benzocyclobutene (flip chip bump process) |
| BDR     | Basic data rate                           |
| BER     | Bit error rate                            |
| BOM     | Bill of materials                         |
| BR      | Baud rate                                 |
| BRF     | Bluetooth RF unit                         |
| BSS     | Basic service set                         |
| BSSID   | Basic service set identifier              |
| BTM     | BSS transition management                 |
| BTU     | Bluetooth baseband unit                   |
| BWQ     | Bandwidth queue                           |
| CBC     | Cipher block chaining                     |
| CBP     | Contention-based period                   |

Table 57. Acronyms and abbreviations...continued

| Acronym | Definition                                          |
|---------|-----------------------------------------------------|
| CCA     | Clear channel assessment                            |
| CCK     | Complementary code keying                           |
| CCMP    | Counter mode CBC-MAC protocol                       |
| CDE     | Close descriptor enable                             |
| CFP     | Contention-free period                              |
| CFQ     | Contention-free queue                               |
| CID     | Connection identifier                               |
| CIS     | Card information structure                          |
| CIU     | CPU interface unit                                  |
| CMD     | Command                                             |
| CMQ     | Control management queue                            |
| CRC     | Cyclic redundancy check                             |
| CS      | Card select                                         |
| CSL     | Coordinated sampled listening                       |
| CSMA/CA | Carrier sense multiple access / collision avoidance |
| CSMA/CD | Carrier sense multiple access / collision detection |
| CSU     | Clocked serial unit                                 |
| CTS     | Clear to send                                       |
| DAC     | Digital-to-analog converter                         |
| DBPSK   | Differential binary phase shift keying              |
| DCD     | Device controller driver                            |
| DCE     | Data communication equipment                        |
| DCF     | Distributed coordination function                   |
| DCLA    | Direct current level adjustment                     |
| DCLB    | Digital contactless bridge                          |
| DCU     | DMA controller unit                                 |
| DFS     | Dynamic frequency selection                         |
| DIFS    | Distributed inter frame space                       |
| DMA     | Direct memory access                                |
| DPD     | Digital pre distortion                              |
| dQH     | Device queue head                                   |
| DQPSK   | Differential quadrature phase shift keying          |
| DSM     | Distribution system medium                          |
| DSP     | Digital signal processor                            |
| DSRC    | Dedicated short range communications                |
| dTD     | Linked list transfer descriptors                    |

Table 57. Acronyms and abbreviations...continued

| Acronym  | Definition                                                   |
|----------|--------------------------------------------------------------|
| DTIM     | Delivery traffic indication message                          |
| DUP      | Duplicated packet                                            |
| DVSC     | Digital voltage scaling control                              |
| EAP      | Extensible authentication protocol                           |
| EBRAM    | Extended block random access memory                          |
| ECDSA    | Elliptic curve digital signature algorithm                   |
| ED       | Energy detect                                                |
| EDCA     | Enhanced distributed channel access                          |
| EEPROM   | Electrically erasable programmable read only memory          |
| EIFS     | Extended inter frame Space                                   |
| ELS      | Embedded Edgelock® secure subsystem                          |
| EMC      | Electromagnetic compatibility                                |
| ER       | Extended range                                               |
| ERP-OFDM | Extended rate PHY-orthogonal frequency division multiplexing |
| ETSI     | European telecommunications standards institute              |
| eWLP     | Embedded wafer level package                                 |
| FCC      | Federal communications commission                            |
| FIFO     | First in first out                                           |
| FIPS     | Federal information processing standards                     |
| FIQ      | Fast interrupt request                                       |
| FPU      | Floating point unit                                          |
| FW       | Firmware                                                     |
| GATT     | Generic attribute profile                                    |
| GCMP     | Galois/counter mode protocol                                 |
| GI       | Guard interval                                               |
| GPIO     | General purpose input/output                                 |
| GPL      | General Public License                                       |
| GPT      | General purpose timer                                        |
| GPU      | General purpose input/output unit                            |
| HID      | Human interface device                                       |
| HIU      | Host interface unit                                          |
| HOGP     | HID over GATT profile                                        |
| HSP      | Hands-free profile                                           |
| HT       | High throughput                                              |
| HVQFN    | Thermal enhanced very thin quad flat package                 |
| HW       | Hardware                                                     |

Table 57. Acronyms and abbreviations...continued

| Acronym | Definition                                        |
|---------|---------------------------------------------------|
| I/F     | Interface                                         |
| I/Q     | In-phase/quadrature                               |
| IB      | In band                                           |
| ICE     | In-circuit emulator (or emulation)                |
| ICR     | Interrupt cause register                          |
| ICU     | Interrupt controller unit                         |
| ICV     | Integrity check value                             |
| IE      | Information element                               |
| IEEE    | Institute of electrical and electronics engineers |
| IEMR    | Interrupt event mask register                     |
| IFS     | inter frame space                                 |
| IMR     | Interrupt mask register                           |
| IPG     | Inter-packet gap                                  |
| IPsec   | Internet protocol security                        |
| IR      | Infrared                                          |
| IRQ     | Interrupt request                                 |
| ISA     | Instruction set architecture                      |
| ISDN    | Integrated services digital network               |
| ISM     | Industrial, scientific, and medical               |
| ISMR    | Interrupt status mask register                    |
| ISR     | Interrupt status register                         |
| JEDEC   | Joint electronic device engineering council       |
| JTAG    | Joint test action group                           |
| LC3     | Low complexity communication codec                |
| LDPC    | Low density parity check                          |
| LE      | Low energy                                        |
| LED     | Light emitting diode                              |
| LME     | Layer management entity                           |
| LNA     | Low noise amplifier                               |
| LPM     | Low power management                              |
| LSb     | Least significant bit                             |
| LSB     | Least significant byte                            |
| LSP     | Low-speed peripheral                              |
| LTE     | Long term evolution                               |
| MAC     | Media/medium access controller                    |
| MC      | Memory controller                                 |

Table 57. Acronyms and abbreviations...continued

| Acronym | Definition                                           |
|---------|------------------------------------------------------|
| MCI     | Microcontroller subsystem                            |
| MCS     | Modulation and coding scheme                         |
| MCU     | MAC Control unit                                     |
| MDI     | Modem data interface                                 |
| MIB     | Management information base                          |
| MIC     | Message integrity code                               |
| MII     | Media independent interface                          |
| MIMO    | Multiple input multiple output                       |
| MIPS    | Million instructions per second                      |
| MLME    | MAC sublayer management entity                       |
| MMI     | Modem management interface                           |
| MMPDU   | MAC management protocol data unit                    |
| MMU     | Memory management unit                               |
| MPDU    | MAC protocol data unit                               |
| MPU     | Memory protection unit                               |
| MSb     | Most significant bit                                 |
| MSB     | Most significant byte                                |
| MSDU    | MAC service data unit                                |
| MU-MIMO | Multi user MIMO                                      |
| MU-PPDU | Multi user PPDU                                      |
| MWS     | Mobile wireless system<br>Multimedia wireless system |
| NAV     | Network allocation vector                            |
| NBS     | Narrow band speech                                   |
| NDP     | Null data packet                                     |
| NL      | No load                                              |
| NPTR    | Next descriptor pointer                              |
| Nsts    | Number of space time streams                         |
| NVIC    | Nested vector interrupt controller                   |
| OCB     | Outside the context of a BSS                         |
| OFDM    | Orthogonal frequency division multiplexing           |
| OID     | Object identifier                                    |
| OOB     | Out of band                                          |
| OTP     | One time programmable                                |
| OTT     | Over-the-top (device)                                |
| P2P     | Peer-to-peer                                         |

Table 57. Acronyms and abbreviations...continued

| Acronym | Definition                        |
|---------|-----------------------------------|
| PA      | Power amplifier                   |
| PAD     | Packet assembler/disassembler     |
| PBU     | Peripheral bus unit               |
| PC      | Point coordinator                 |
| PCB     | Printed circuit board             |
| PCF     | Point coordination function       |
| PCI     | Peripheral component interconnect |
| PCIe    | PCI express                       |
| PCM     | Pulse code modulation             |
| PDn     | Power down                        |
| PDU     | Protocol data unit                |
| PEAP    | Protected EAP                     |
| PHY     | Physical layer                    |
| PIFS    | Priority inter frame space        |
| PLL     | Phase-locked loop                 |
| PLME    | Physical layer management entity  |
| PMU     | Power management unit             |
| POS     | Point of sale                     |
| POST    | Power-on self test                |
| PPDU    | PHY protocol data unit            |
| PPK     | Per-packet key                    |
| PPM     | Pulse position modulation         |
| PSK     | Pre shared keys                   |
| PTA     | Packet traffic arbitration        |
| PUF     | Physically unclonable function    |
| PWK     | Pairwise key                      |
| QAM     | Quadrature amplitude modulation   |
| QFN     | Quad flat non-leaded package      |
| QoS     | Quality of service                |
| RA      | Receiver address                  |
| RBDS    | Radio broadcast data system       |
| RDS     | Radio data system                 |
| RF      | Radio frequency                   |
| RFID    | Radio frequency identification    |
| RIFS    | Reduced inter frame space         |
| RISC    | Reduced instruction set computer  |

Table 57. Acronyms and abbreviations...continued

| Acronym | Definition                           |
|---------|--------------------------------------|
| ROM     | Read only memory                     |
| RSSI    | Receiver signal strength indication  |
| RTC     | Real time clock                      |
| RTS     | Request to send                      |
| RTU     | General purpose timer unit           |
| RU      | Resource unit                        |
| SA      | Source address                       |
| SAP     | Service access point                 |
| SCLK    | Serial interface clock               |
| SDA     | Serial interface data                |
| SDK     | Software development kit             |
| SE      | Secure element                       |
| SFD     | Start of frame delimiter             |
| SHA     | Secure hash algorithm                |
| SIFS    | Short inter frame space              |
| SISO    | Single input single output           |
| SIU     | Serial interface unit (UART)         |
| SJU     | System/software JTAG controller unit |
| SM      | Switch module                        |
| SMI     | Serial management interface          |
| SNR     | Signal-to-noise ratio                |
| SO      | Serial out                           |
| SoC     | System-on-chip                       |
| SPDT    | Single pole double throw             |
| SPI     | Serial peripheral interface          |
| SQU     | Internal SRAM unit                   |
| SRWB    | Serial interface read write          |
| SS      | Service set                          |
| SSID    | Service set identifier               |
| STA     | Station                              |
| STBC    | Space-time block code                |
| SWD     | Serial wire debug                    |
| SWP     | Single wire protocol                 |
| SysTick | System tick timer                    |
| TA      | Transmitter address                  |
| TBG     | Time base generator                  |

Table 57. Acronyms and abbreviations...continued

| Acronym  | Definition                                                       |
|----------|------------------------------------------------------------------|
| TBTT     | Target beacon transmission time                                  |
| TCM      | Tightly coupled memory                                           |
| TCP/IP   | Transmission control protocol/internet protocol                  |
| TCQ      | Traffic category queue                                           |
| TEE      | Trusted execution environment                                    |
| TIM      | Traffic indication map                                           |
| TKIP     | Temporal key integrity protocol                                  |
| TPC      | Transmit power control                                           |
| TQFP     | Thin quad flat pack                                              |
| TRPC     | Transmit rate-based power control                                |
| TSF      | Timing synchronization function                                  |
| TWT      | Target wait time                                                 |
| UART     | Universal asynchronous receiver/transmitter                      |
| USART    | Universal synchronous/asynchronous receiver/transmitter          |
| UBM      | Under bump metal                                                 |
| UDP      | User datagram protocol                                           |
| UNII     | Unlicensed national information infrastructure                   |
| VCO      | Voltage controlled oscillator                                    |
| VHT      | Very high throughput                                             |
| VIF      | Voice interface                                                  |
| WAP      | Wireless application protocol                                    |
| WAVE     | Wireless access in vehicular environments                        |
| WBS      | Wide band speech                                                 |
| WCI-2    | Wireless coexistence interface 2                                 |
| WEP      | Wired equivalent privacy                                         |
| WFI      | Wait for interrupt                                               |
| WI       | Wired interface                                                  |
| Wi-Fi    | Hardware implementation of IEEE 802.11 for wireless connectivity |
| WLAN     | Wireless local area network                                      |
| WLCSP    | Wafer level chip scale package                                   |
| WMM      | Wi-Fi multimedia                                                 |
| WPA      | Wi-Fi protected access                                           |
| WPA2     | Wi-Fi protected access 2                                         |
| WPA2-PSK | Wi-Fi protected access 2 - pre shared key                        |
| WPA3     | Wi-Fi protected access 3                                         |
| WPA-PSK  | Wi-Fi protected access - pre shared key                          |

Table 57. Acronyms and abbreviations...continued

| Acronym | Definition                  |
|---------|-----------------------------|
| XIP     | Execute in place            |
| XOSC    | Crystal oscillator          |
| ZIF     | Zero intermediate frequency |

## 12 Revision history

Table 58. Revision history

| Document ID       | Release date                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Data sheet status        | Change notice | Supersedes        |
|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|---------------|-------------------|
| 88W8987_SDS v.6.0 | 20221202                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Product short data sheet | -             | 88W8987_SDS v.5.0 |
| Modifications     | <b>Bluetooth subsystem</b> <ul style="list-style-type: none"> <li><a href="#">Section 4.1 "2.4 GHz Bluetooth Tx/Rx"</a>: added a note to <i>AES encryption</i> feature</li> <li><a href="#">Section 4.2 "Bluetooth Low Energy (LE)"</a>: added a note to <i>AES encryption</i> and <i>Bluetooth LE Secure Connection</i> features</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                          |               |                   |
| 88W8987_SDS v.5.0 | 20221111                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Product short data sheet | -             | 88W8987_SDS v.4.0 |
| Modifications     | <b>Electrical specifications</b> <ul style="list-style-type: none"> <li><a href="#">Section 9.3.4 "2.4 GHz Wi-Fi transmitter performance"</a>: added <math>\pm</math> to <i>Transmit output power accuracy</i> typical value</li> <li><a href="#">Section 9.3.5 "5 GHz Wi-Fi transmitter performance"</a>: added <math>\pm</math> to <i>Transmit output power accuracy</i> typical value</li> <li><a href="#">Section 9.4.2 "Bluetooth and Bluetooth LE transmitter performance"</a>: added <i>Transmit power accuracy</i> typical value</li> <li><a href="#">Section 9.5 "Current consumption"</a>: <ul style="list-style-type: none"> <li>Updated the note above the table</li> <li>Added the column and values for VIO_3.3 V</li> <li>Added the rows and values for Wi-Fi 2.4 GHz receive idle mode</li> <li>Added the rows and values for Wi-Fi 5 GHz receive idle mode</li> <li>Updated <i>Maximum peak current consumption during device initialization</i> values and conditions</li> </ul> </li> </ul> |                          |               |                   |
| 88W8987_SDS v.4.0 | 20220503                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Product short data sheet | -             | 88W8987_SDS v.3.0 |
| Modifications     | <b>Electrical specifications</b> <ul style="list-style-type: none"> <li><a href="#">Section 9.5 "Current consumption"</a>: updated the values for sleep mode</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                          |               |                   |
| 88W8987_SDS v.3.0 | 20210915                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Product short data sheet | -             | 88W8987_SDS v.2.0 |
| Modifications     | <ul style="list-style-type: none"> <li>Removed the content about WEP and TKIP as these encryption methods are no longer supported. Updated sections: <ul style="list-style-type: none"> <li><a href="#">Section 1 "Product overview"</a></li> <li><a href="#">Section 1.2 "Wi-Fi key features"</a></li> <li><a href="#">Section 3.5 "Wi-Fi encryption"</a></li> </ul> </li> <li><a href="#">Section 9.8.1 "PCM interface specifications"</a>: <ul style="list-style-type: none"> <li>PCM_CLK in <a href="#">Figure 20</a> and <a href="#">Figure 22</a>: renamed T<sub>BCLK</sub> as 1/F<sub>BCLK</sub>, added T<sub>BCLK</sub> rise and T<sub>BCLK</sub> fall</li> <li><a href="#">Table 42</a> and <a href="#">Table 43</a>: added F<sub>BCLK</sub> min and max values</li> </ul> </li> </ul>                                                                                                                                                                                                                |                          |               |                   |
| 88W8987_SDS v.2.0 | 20210521                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Product short data sheet | -             | 88W8987_SDS v.1.0 |
| Modifications     | <ul style="list-style-type: none"> <li>Updated Bluetooth certification compliance to version 5.2</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                          |               |                   |
| 88W8987_SDS v.1.0 | 20201008                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Product short data sheet | -             | -                 |

## 13 Legal information

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| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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