

Internal Clock Source (ICS) Module on the HCS08s in Depth

by: Scott Pape
Systems Engineering, Freescale Microcontroller Division

In this document, we will take a closer look at the internal clock source module (ICS) that can be found on some members of the HCS08 Family of microcontrollers (MCU). The ICS module is a very flexible clock source for the HCS08 MCUs, yet is still cost-effective for use on the smaller, lower cost range of MCUs in this family.

The ICS includes a frequency-locked loop, internal clock reference, external oscillator, and clock selection sub-modules. These sub-modules combine to offer a variety of clock modes and frequencies to meet just about any application. The ICS operates in one of seven modes that will be described in more detail.

Also, we will compare the ICS module to the internal clock generator (ICG) module found on other HCS08s. In addition, we will describe how the ICS module behaves when recovering from the different low power modes of the HCS08s. To conclude, we will cover calibration of the internal clock reference.

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1 ICS Functional Description

In this section we will look at the details of the functional operation of the internal clock source.

1.1 Block Diagram

Figure 1 shows the block diagram for the ICS. The ICS is composed of four main sub-modules:

- Frequency-locked loop (FLL)
- Internal reference clock
- External oscillator
- Clock select logic

The main output of the ICS is ICSOUT. This is the clock signal that is used to generate the CPU and bus clocks. The CPU clock frequency is equal to the ICSOUT frequency and the bus clock frequency is 1/2 of ICSOUT.

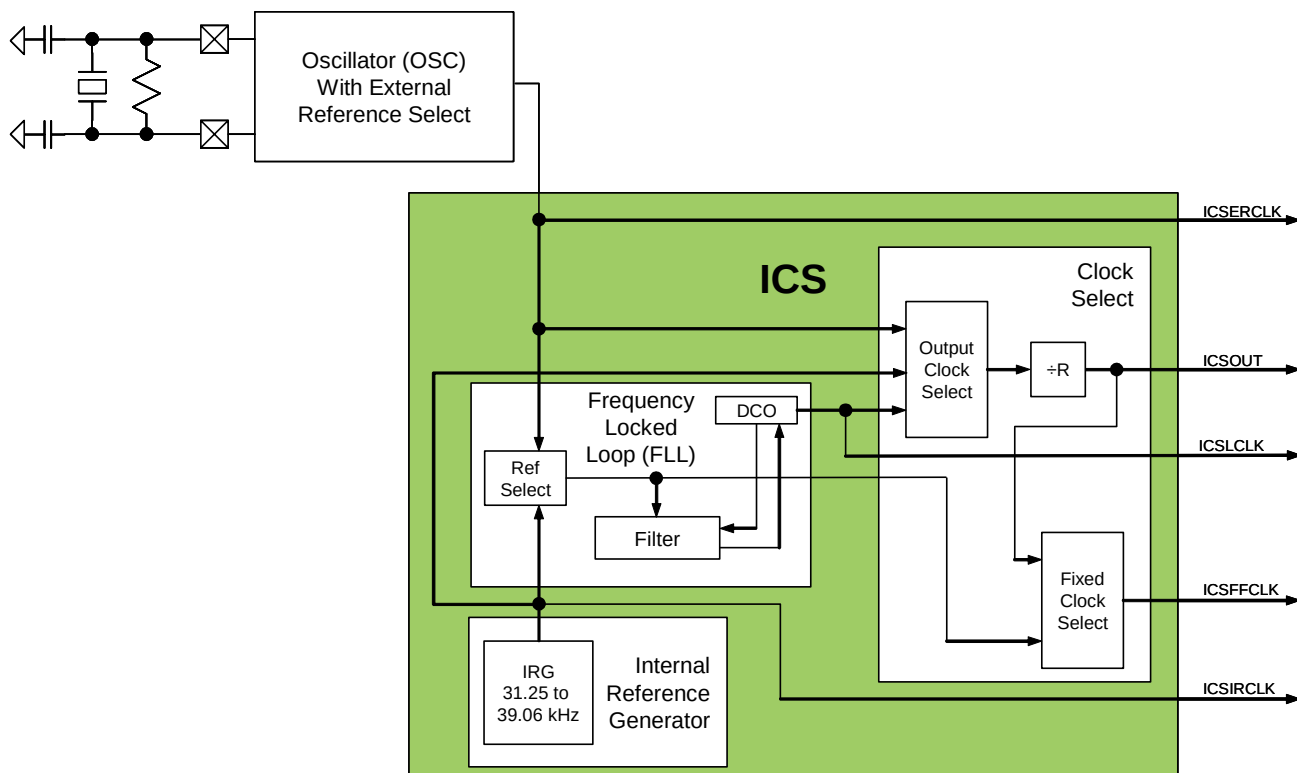


Figure 1. ICS Block Diagram

The FLL outputs a frequency that is 512 times faster than the reference clock frequency. The FLL is composed of three main blocks:

- Reference select
- Digitally-controlled oscillator (DCO)
- Filter which compares the output of the other two blocks

The FLL is very similar in operation to a phase-locked loop (PLL). The difference is that a PLL adjusts the output based on phase differences between the reference clock and the DCO clock, while the FLL works by comparing the frequency of the DCO clock to the reference clock. The FLL counts the number of DCO clock edges during one period of the reference clock. So for the multiplier of 512, the FLL should count 512 rising edges of the DCO between each rising edge of the reference clock. The FLL is implemented with mostly digital logic, eliminating the need for external filter components typically needed on a PLL.

The clock select logic simply selects the output of the FLL, the external clock reference, or the internal clock reference as the output of the ICS module. In addition, a clock divider circuit is included to reduce the output clock frequency by dividing the output by 1, 2, 4, or 8.

The internal reference clock (IRC) is a trimmable internal reference that can be used either as the reference clock for the FLL or directly as the source for the CPU and bus clocks. This internal reference requires no external components such as trimming capacitors or resistors. The IRC is trimmed by a 9-bit value in the ICS registers, which gives a typical resolution of 0.1% of the IRC's untrimmed frequency. Unlike many other internal references, this IRC can be trimmed to a range of frequencies, from 31.25 kHz to 39.06 kHz. When used as the FLL reference, this allows the user to set the bus frequency anywhere from 8 MHz to 10 MHz with 0.1% resolution. After trimming, the typical deviation from the trimmed frequency is only +0.5% to -1% typical and only $\pm 2\%$ maximum.

The external oscillator reference (OSC) is actually three external clock sources combined into one. It has a low-frequency oscillator for use with 32 kHz to 38.4 kHz crystals or resonators. It has a high-frequency oscillator for use with 1 MHz to 16 MHz crystals or resonators. Both of these oscillators require two pins, XTAL and EXTAL to generate the clock signal. The OSC also has an external clock mode which simply passes an external clock signal into the MCU. In this mode, only the EXTAL pin is required and the XTAL pin can be used as general I/O. The input frequency can be anywhere from 0 Hz to 20 MHz. Due to pin limitations, some MCUs may not have an external oscillator.

Which ICS sub-modules are actually active depends on the selected clock mode of the ICS. The ICS has seven modes of operation:

- Off
- FLL engaged, internal reference (FEI)
- FLL engaged, external reference (FEE)
- FLL bypassed, internal reference (FBI)
- FLL bypassed, internal reference, low power (FBILP)
- FLL bypassed, external reference (FBE)
- FLL bypassed, external reference, low power (FBELP)

1.2 ICS Modes: Off

The ICS is turned off when one of the MCU's low power stop modes is entered. In off mode, the FLL is always disabled to conserve power. However, there are options to keep the external reference, internal reference, or both, enabled in stop3 mode. This feature allows certain modules to operate in stop3, such as the real-time interrupt (RTI) module, which can use the external reference as its clock reference. Some MCUs may not have modules that are connected to the internal and/or external reference. For lowest power operation, the reference clocks should be disabled if not needed.

1.3 ICS Modes: FEI

The FLL engaged, internal reference (FEI) mode is the default mode after any chip reset, including power-on reset (POR). In this mode, the FLL is active and the output drives the CPU and bus clocks. The IRC is used as the reference frequency for the FLL, so absolutely no external components (such as filter caps or trimming resistors) are required and the EXTAL and XTAL pins can be used for alternate functions.

The bus frequency in FEI can be calculated from [Equation 1](#):

$$f_{bus} = f_{IRC} \times 512 \div (2 \times \text{bus divider}) \quad \text{Eqn. 1}$$

Because the internal reference can be trimmed to a range of frequencies from 31.25 kHz to 39.06 kHz, FEI mode will generate frequencies 512 times faster; i.e., from 16 MHz to 20 MHz. After any reset, the clock divider, mentioned above and described in more detail later, will add an extra divide-by-2 to ICSOUT. This is to protect the system in the event that the IRC is untrimmed and running faster than 31.25 kHz. This would result in a bus frequency greater than 8 MHz, which is outside the MCU's low voltage (<2.1 V) maximum frequency specification. By defaulting to divide-by-2, the bus frequency is guaranteed to be within spec for any operating voltage range, but is still fast enough to allow for rapid configuration of the MCU.

The internal reference should be trimmed after any POR because this resets the trim value to 0x80 and the fine trim bit to 0. All other resets leave the current trim value as is.

1.4 ICS Modes: FEE

In the FLL engaged, external reference (FEE) mode, the FLL is active and the output drives the CPU and bus clocks. The external oscillator provides the reference clock to the FLL. The FLL output needs to be in the range of 16 MHz to 20 MHz for proper system operation. Therefore, there are limits on the frequency of the external reference when FEE mode will be used. The ICS includes a reference divider that can be used to reduce the frequency of the external reference to allow for more external clock options. The reference divider is selected by the RDIV bits in the ICS control register 1 (ICSC1). [Table 1](#) shows the allowable external frequencies based on the RDIV setting.

Table 1. Allowable External Frequencies for FEE Mode

RDIV	Divide By...	Minimum External Frequency (MHz)	Maximum External Frequency (MHz)
000	1	0.03125	0.03906
001	2	0.0625	0.07812
010	4	0.125	0.1562
011	8	0.25	0.3125
100	16	0.50	0.625
101	32	1.0	1.25
110	64	2.0	2.5
111	128	4.0	5.0

The bus frequency in FEE can be calculated from [Equation 2](#):

$$f_{bus} = (f_{OSC} \div \text{reference divider}) \times 512 \div (2 \times \text{bus divider}) \quad \text{Eqn. 2}$$

1.5 ICS Modes: FBI and FBILP

The FLL bypassed, internal reference (FBI) and FLL bypassed, internal reference, low power (FBILP) modes are identical except for one difference. Both modes bypass the FLL and use the IRC directly to generate ICSOUT. The difference is that FBI mode keeps the FLL active and FBILP disables the FLL, thereby saving additional power. FBILP is enabled by configuring for FBI and setting the LP bit in the ICS control register 2 (ICSC2).

A couple of reasons for using FBI instead of FBILP are one, to use background debug mode (BDM) or two, to save FLL lock time if the application will be switching to FEI. The FLL must be active to provide a high speed clock source for BDM communication. If the LP bit is set while the BDM is enabled, then the FLL will remain active despite the LP bit setting. Also, if the BDM becomes enabled after the LP bit has been set, the FLL will switch on. The FLL lock time has a maximum spec of 1 ms and typically requires about 500 μ s. Disabling the FLL typically saves about 220–310 μ A, depending on V_{DD} and the FLL frequency.

1.6 ICS Modes: FBE and FBELP

The FLL bypassed, external reference (FBE) and FLL bypassed, external reference, low power (FBELP) modes are similar to the FBI and FBILP modes described above except that the OSC is used to generate the clock source instead of the IRC. The FLL is still bypassed as in FBI/FBILP and the LP bit is used to disable the FLL if BDM is not enabled.

In [Section 1.4](#), we saw that the OSC frequencies are limited when the FLL is engaged (FEE). If FEE mode will not be used and the ICS is put in FBELP mode (remember, the FLL is still active in FBE mode), then

these restrictions are lifted and the only restrictions are the limits of the OSC reference itself: low-frequency oscillator from 32 kHz to 38.4 kHz, high-frequency oscillator from 1 MHz to 16 MHz, and external clock mode from 0 Hz to 20 MHz. However, if the BDM will be enabled, then the FEE oscillator restrictions do apply in FBILP.

Also, the reference divider discussed in [Section 1.4](#) has no effect while in FBELP. The oscillator restrictions from FEE mode do apply in FBE mode.

1.7 ICS vs. ICG

Several HCS08 MCUs are currently available with an internal clock generator (ICG) module. There are several distinctions that should be made to differentiate the ICS from the ICG. Although the ICS is an entirely new module, it is basically a subset of the ICG in regards to functionality. The purpose of the ICS is to offer a smaller, lower power clock module for the smaller, more cost sensitive HCS08 MCUs.

First, the FLL in the ICG module has more options for generating the output frequency. Where the ICS FLL is fixed at a multiplier of 512 for output frequencies of 16 MHz to 20 MHz, the ICG FLL has eight software selectable multiplier values, plus an additional prescaler for using both high frequency (> 1 MHz) and low frequency (<100 kHz) clock references. The ICG FLL can output frequencies from 8 MHz to 40 MHz with fewer restrictions on the reference clock.

The ICG provides more clock status bits. The ICG provides nine status bits for monitoring just about all facets of the ICG operation, including LOCK status, current ICG mode, DCO stability, and external reference stability (among others). The ICS has three status bits: two to monitor the current ICS mode, and one bit for indicating the external oscillator has been initialized.

The ICG also includes a clock monitor circuit that makes provisions for resets or interrupts when the FLL loses lock or a clock source is lost. Not only will a loss-of-clock or loss-of-lock generate either a reset or interrupt, but the ICG will switch to an internal clock source to maintain CPU operation. The ICS has no features for monitoring either loss-of-clock or loss-of-lock. However, some HCS08 MCUs do provide a completely independent clock source for the COP watchdog timer that can reset the MCU if the CPU and bus clocks are corrupted.

More details on the ICG can be found in the data sheet for any HCS08 MCU with an ICG module, such as the MC9S08GB60, or in application note AN2494.

1.8 Additional Application Features

A couple of additional features that should be mentioned are the bus divider and the high gain oscillator.

The bus divider has been mentioned earlier in this document. The bus divider has four software selectable values for dividing the bus clock: 1, 2, 4, or 8, selectable by the BDIV bits in ICSC2. It is available in all ICS modes except off mode. It is useful for reducing the CPU and bus clocks when higher bus speeds are not necessary, thereby reducing power consumption. The divider is outside of the FLL, so changing the value does not cause the FLL to lose lock. Also, the divider simply selects one of four outputs from a divider chain, so the change in frequency occurs in a few bus cycles. Out of any reset, BDIV is set for divide-by-2.

The OSC module has the option to run in a low power or a high gain mode when driving a crystal or resonator. The low-power mode limits the voltage swings on the external components to conserve power. The high gain mode drives the external components from rail-to-rail, making the oscillator circuit less susceptible to board-level noise. The power increase from using the high gain option is dependent on the supply voltage and the OSC frequency. As an example, a 32 kHz crystal running in low-power mode consumes 5 μ A typically and does not vary significantly with V_{DD} . The same crystal running in high gain mode will consume about 40-50 μ A at a V_{DD} of 3 V and the current will vary more with V_{DD} .

2 ICS in Low Power Modes

It is important to understand how the low-power modes affect the operation of the ICS.

2.1 Stop1 and Stop2

The ICS will always be put into off mode when the MCU enters stop1 or stop2. Therefore, the mode the ICS is in when executing the STOP instruction is irrelevant and will have no effect on the power consumption during stop1 or stop2.

Because both stop1 and stop2 result in the MCU executing a POR upon stop recovery, the ICS will always reset to FEI, BDIV set for divide-by-2 for roughly a 4 MHz bus clock. ICSTRM will be reset to 0x80 and the FTRIM bit will be cleared, so if the internal reference will be used, it should either be recalibrated or if the trim value has been saved in FLASH memory, then the saved value needs to be reloaded into the ICS registers.

2.2 Stop3

Most of the ICS will be disabled upon entering stop3, including the FLL. The mode the ICS is in when executing the STOP instruction will not impact the stop3 power consumption. However, two control bits in the ICS will impact the stop3 current, IREFSTEN and EREFSTEN. When set, IREFSTEN causes the IRC to remain enabled in stop3 mode. Similarly, when set, EREFSTEN causes the OSC to remain enabled in stop3. Setting IREFSTEN will result in a stop3 current of roughly 100 μ A. Setting EREFSTEN will have a wide impact on stop3 current depending on the OSC frequency and settings.

If stop3 is exited by a reset, then the ICS will revert to FEI mode just as a stop1 or stop2 recovery. The one exception is that the trim value will not be reset unless a POR has occurred.

If stop3 is exited by an interrupt, then the ICS mode upon stop recovery is determined by the mode when entering stop3:

- In FBI mode, ICS startup is immediate at the trimmed frequency.
- In FEI mode, startup is immediate at the pre-stop, trimmed frequency
- In FEE mode, startup is immediate at pre-stop frequency in open loop mode until stabilization time and then switch to external reference

- In FBE mode, startup is delayed based on the external reference stabilization time. If a crystal or resonator is being used, then the ICS will wait for 4096 oscillator cycles before enabling ICSOUT. If the EREFSTEN bit is set, then this delay is bypassed. Also, if an external clock is being used, then the 4096 cycle delay is bypassed.

NOTE

The term “immediate” refers to a point when the on-chip voltage regulator common on HCS08 MCUs has restarted and is at full regulation. The time for the regulator to recover from stop3 is typically 100-120 μ s from the interrupt signal to CPU operation.

2.3 Wait

Wait mode has no effect on the ICS operation. The ICS will continue in the mode it is in when the WAIT instruction is executed. Recovery from wait mode will also have no effect on the ICS operation unless a reset occurred, the ICS will reset as described above.

3 Calibrating the IRC

The IRC in the ICS will require trimming if FEI or FBI modes will be used since the FLL is active in these modes. To keep the FLL output within the spec limits of 16 MHz to 20 MHz, the IRC frequency needs to be between 31.25 kHz and 39.06 kHz. In FBILP, the FLL is disabled and therefore trimming the IRC is optional.

3.1 How to Calibrate — AN2496

AN2496, *Calibrating the MC9S08GB/GT Internal Clock Generator (ICG)*, discusses trimming of the internal reference generator in the ICG module. Trimming the IRC in the ICS is basically the same. Therefore, for details on in-circuit trimming methods, please read AN2496. The software examples presented in AN2496 can easily be modified to work with MCUs having an ICS instead of an ICG.

3.2 Untrimmed Operation

After a POR, the ICS is in its default mode of FEI with the BDIV set for divide-by-2. The ICSTRM value will be reset to 0x80 and the FTRIM bit will be cleared. This puts the 9-bit trim value right in the middle of its range. Due to fab processing variations, the frequency of the of the IRC will range from 25 kHz to 41.66 kHz. Using [Equation 1](#), the resulting bus frequency range is therefore 3.2 MHz to 5.33 MHz.

The ICS can operate without issues in this untrimmed mode, however, for best results, the IRC should be trimmed.

3.3 Calibrating the IRC

The IRC is calibrated by writing to the ICSTRM register first, then using the FTRIM bit to “fine tune” the frequency. We will refer to this total 9-bit value as the trim value, ranging from 0x000 to 0x1FF, where the FTRIM bit is the LSB.

The trim value after a POR is always 0x100. Writing a larger value will decrease the frequency and smaller values will increase the frequency. As described in AN2496, the trim value is linear with the period, except that slight variations in wafer fab processing produce slight non-linearities between trim value and period. These non-linearities are why AN2496 recommends an iterative trimming approach to search for the best trim value.

After a trim value has been found for a device, this value can be stored in FLASH memory to save the value. If power is removed from the device, the IRC can easily be re-trimmed by copying the saved value from FLASH to the ICS registers. Freescale identifies recommended FLASH locations for storing the trim value for each MCU. Consult the memory map in the data sheet for the specific device for these locations. On devices that are factory trimmed, the factory trim value will be stored in these locations.

How to Reach Us:

Home Page:

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E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

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