Application Note

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DC Motor with Dead-Time Correction TPU Function Set (DCmDt)

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Functional Overview

The DC Motor with Dead-Time Correction (DCmDt) TPU function set extends the functionality of the DC Motor TPU function set (DCm) by incorporating the dead-time correction technique. Apart from this, its functionality is the same in all other aspects.

The dead-time correction technique requires knowledge of the instantaneous direction of the motor current. In the case of positive motor current the SW1 high-time and SW4 low-time are equal to the calculated high-times and the SW2 and SW3 channels have to control the dead-time. In case of negative motor current the SW2 low-time and SW3 high-time are equal to the calculated high-times and the SW1 and SW4 channels have to control the dead-time. See **Figure 2**.

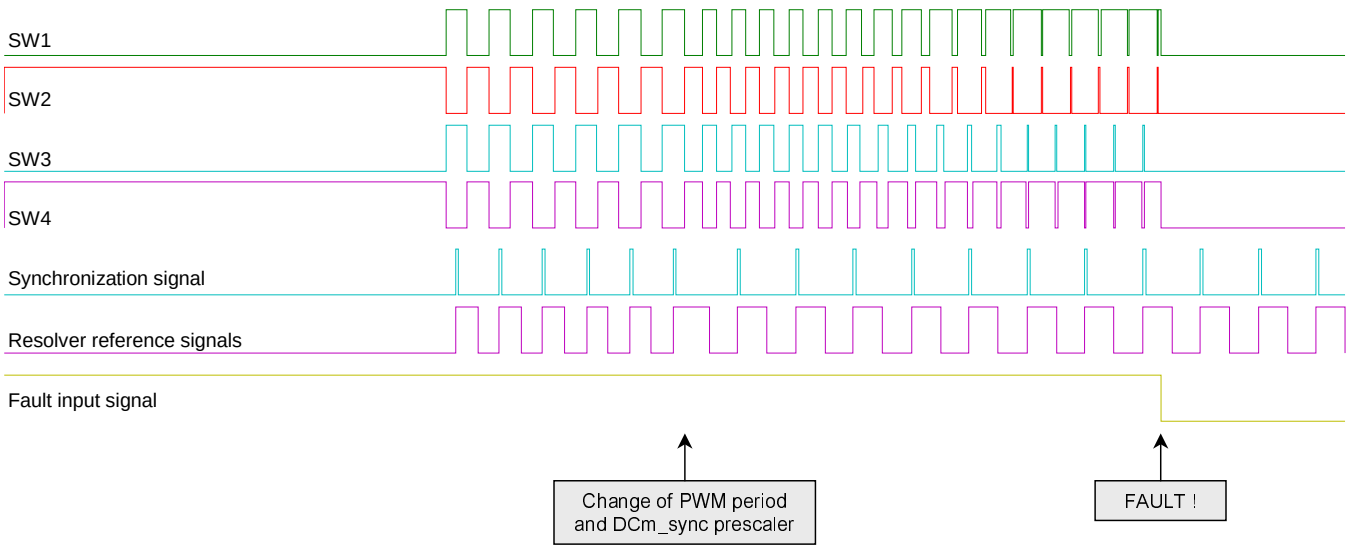

Figure 1. Signals processed by DCmDt TPU function set

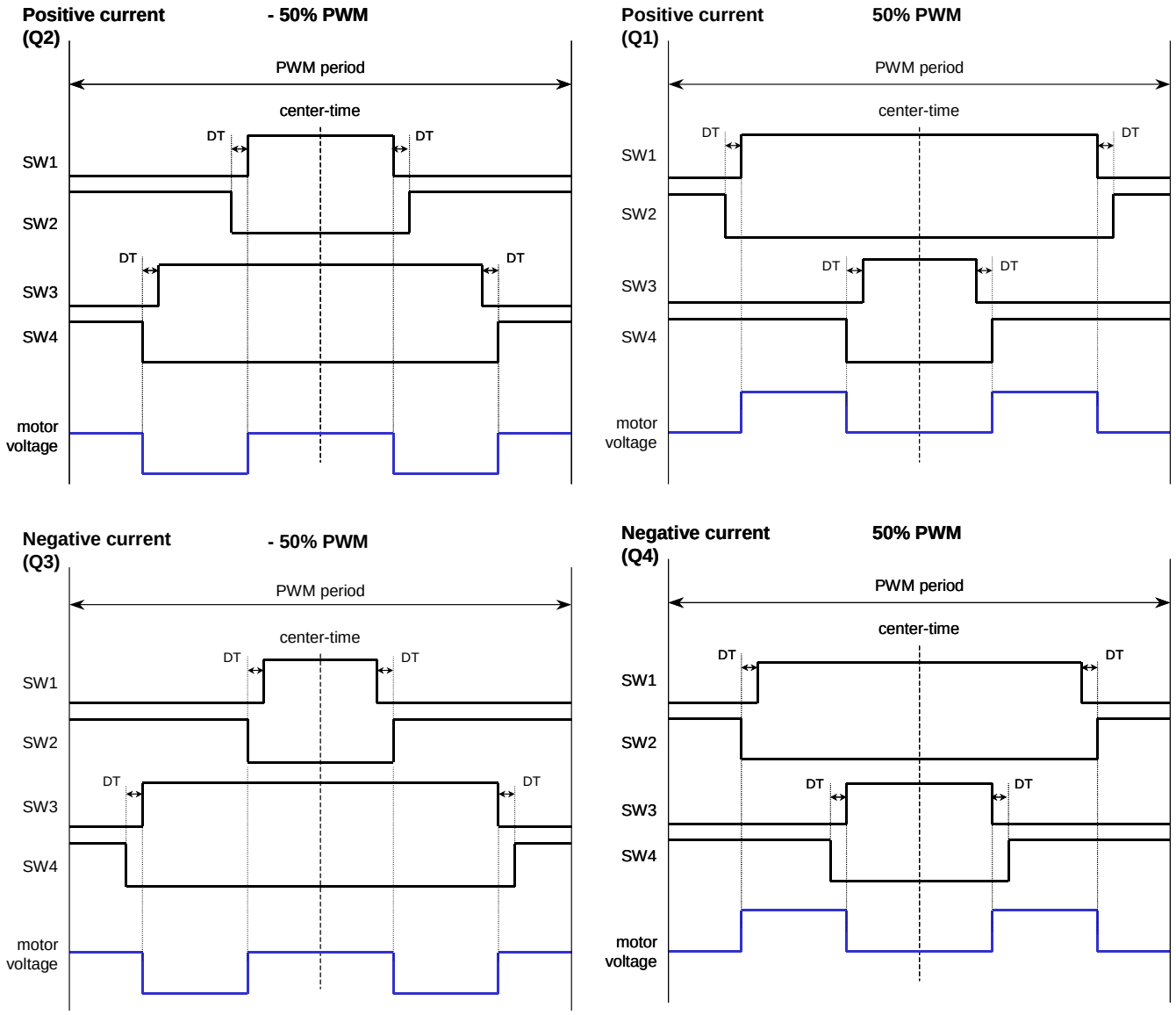

Figure 2. Dead-Time Correction Technique

The DC Motor with Dead-Time Correction TPU function drives a DC Motor, independently of the CPU. The CPU is required only to set the instantaneous direction of the motor current, and a duty-cycle (*dc*) parameter in the range (–1,1). The duty-cycle determines both the motor speed, and direction. The function generates unipolar-switched center-aligned PWM signals.

The function set consists of 4 TPU functions:

- DC Motor with Dead-Time Correction (DCmDt)
- Synchronization Signal for DC Motor with Dead-Time Correction (DCmDt_sync)
- Resolver Reference Signal for DC Motor with Dead-Time Correction (DCmDt_res)
- Fault Input for DC Motor with Dead-Time Correction (DCmDt_fault)

The DCmDt TPU function generates a 4-channel 2-phase center-aligned PWM signal with dead-time between the top and bottom channels. The Synchronization Signal for the DCmDt function can be used to generate one or more adjustable signals for a wide range of uses. These signals are synchronized to the PWM, and track changes in the PWM period. The Resolver Reference Signal for the DCmDt function can be used to generate one or more 50% duty-cycle adjustable signals that are also synchronized to the PWM.The Fault Input for the DCmDt function is a TPU input function that sets all PWM outputs low when the input signal goes low. See **Figure 1**.

Function Set Configuration

The DCmDt function has to be used on 4 output channels, and within each phase, the top channel has to be assigned on a lower TPU channel than the bottom channel. One or more channels running Synchronization Signal for DCmDt as well as Resolver Reference Signals for DCmDt functions can be added. They can run with different settings on each channel. The function Fault Input for DCmDt can also be added. It is recommended to use it on channel 15, and to set the hardware option that disables all TPU output pins when the channel 15 input signal is low (DTPU bit = 1). This ensures that the hardware reacts quickly to a pin fault state. Note that it is not only the PWM channels, but all TPU output channels, including the synchronization signals, that are disabled in this configuration.

Table 1 shows the configuration options and restrictions.

Table 1. DCmDt TPU function set configuration options and restrictions

TPU function	Optional/ Mandatory	How many channels	Assignable channels
DCmDt	mandatory	4	any 4 channels, SW1 on a lower channel then SW2, SW3 on a lower channel then SW4
DCmDt_sync	optional	1 or more	any channels
DCmDt_res	optional	1 or more	any channels
DCmDt_fault	optional	1	any, recommended is 15 and DTPU bit set

Table 2 shows an example of configuration.

Table 2. Example of configuration

Channel	TPU function	Priority
0	DCmDt	high
1	DCmDt	high
2	DCmDt	high
3	DCmDt	high
10	DCmDt_sync	low
11	DCmDt_res	low
15	DCmDt_fault	high

Table 3 shows the TPU function code sizes.

Table 3. TPU function code sizes

TPU function	Code size
DCmDt	116 µ instructions + 8 entries = 124 long words
DCmDt_sync	26 µ instructions + 8 entries = 34 long words
DCmDt_res	38 µ instructions + 8 entries = 46 long words
DCmDt_fault	9 µ instructions + 8 entries = 17 long words

Configuration Order

The CPU configures the TPU as follows.

1. Disables the channels by clearing the two channel priority bits on each channel used (not necessary after reset).
2. Selects the channel functions on all used channels by writing the function numbers to the channel function select bits.
3. Initializes function parameters. The parameters *T*, *DT*, *MPW* and *sync_presc_addr* must be set before initialization. If a DCmDt_sync channel or a DCmDt_res channel is used, then its parameters must also be set before initialization.
4. Issues an HSR (Host Service Request) type %10 to one of the DCmDt channels to initialize all PWM channels. Issues an HSR type %10 to the DCmDt_sync channels, DCmDt_res channels and DCmDt_fault channel, if used.
5. Enables servicing by assigning high, middle or low priority to the channel priority bits. All PWM channels must be assigned the same priority to ensure correct operation. The CPU must ensure that the DCmDt_sync or DCmDt_res function is initialized after the initialization of DCmDt:
   - assign a priority to the PWM channels to enable their initialization
   - if a Synchronization Signal or a Resolver Reference Signal channel is used, wait until the HSR bits are cleared to indicate that initialization of the PWM channels has completed and
   - assign a priority to the DCmDt_sync or DCmDt_res channel to enable its initialization

NOTE: *A CPU routine that configures the TPU can be generated automatically using the MPC500_Quick_Start Graphical Configuration Tool.*

Detailed Function Description

DC Motor with Dead-Time Correction (DCmDt)

The DCmDt TPU function generates a 4-channel, 2-phase unipolar-switched center-aligned PWM signal, with dead-time between the top and bottom channels. In order to charge the bootstrap transistors, the PWM signals start to run 1.6ms after their initialization (at 20MHz TCR1 clock). The functions generate signals corresponding to value 0 in duty-cycle ratio *dc* until the first *dc* value is processed, or for at least one PWM period.

The CPU controls the PWM output by setting the TPU parameters. The duty-cycle ratio *dc*, PWM period *T* and *current* can be adjusted during run time. Conversely, dead-time (*DT*) and minimum pulse width (*MPW*) are not supposed to be changed during run time. The duty-cycle ratio *dc* can gain a value in the range (–1, 1). The sign controls the motion system direction, while the absolute value controls the amplitude of the applied voltage.

The following figures show the input *dc* value and corresponding output PWM signals (valid for positive motor current):

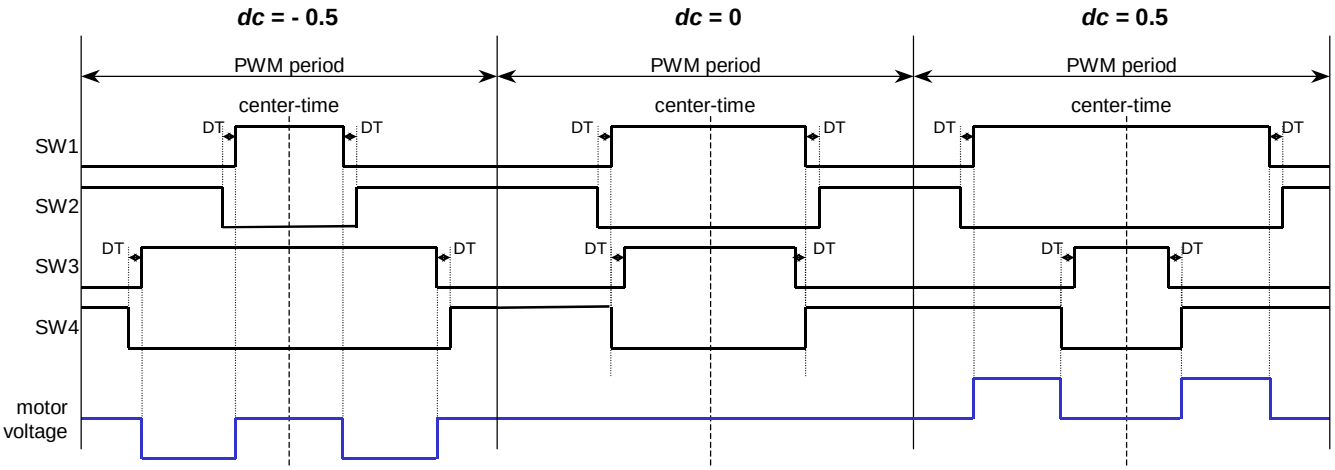

Figure 3. Unipolar switching

The following equations describe how the PWM signal transition times $SW1_{LH}$, $SW2_{LH}$, $SW3_{LH}$, $SW4_{LH}$, $SW1_{HL}$, $SW2_{HL}$, $SW3_{HL}$ and $SW4_{HL}$ are calculated:

$$Tdc = T \cdot dc$$

$$X = \frac{T + Tdc}{2}$$

$$Y = \frac{T - Tdc}{2}$$

Positive current (*current* = 0)

$$A = \frac{X}{2}$$

$$B = \frac{X}{2} + DT$$

$$C = \frac{Y}{2}$$

$$D = \frac{Y}{2} + DT$$

$$SW1_{LH} = center\_time - A$$

$$SW2_{HL} = center\_time - B$$

$$SW3_{LH} = center\_time - C$$

$$SW4_{HL} = center\_time - D$$

Negative current (*current* = 1)

$$A = \frac{X}{2} - DT$$

$$B = \frac{X}{2}$$

$$C = \frac{Y}{2} - DT$$

$$D = \frac{Y}{2}$$

$$SW1_{HL} = center\_time + A$$

$$SW2_{LH} = center\_time + B$$

$$SW3_{HL} = center\_time + C$$

$$SW4_{LH} = center\_time + D$$

Host Interface

Written By CPU

Written by both CPU and TPU

Written By TPU

Not Used

Table 4. DCmDt Control Bits

Name	Options
3 2 1 0 Channel Function Select	DCmDt function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
1 0 Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Stop
1 0 Host Sequence Bits (HSQ)	xx – Not used
0 Channel Interrupt Enable	x – Not used
0 Channel Interrupt Status	x – Not used

Table 5. DCmDt Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW1	0	LHtime_1															
	1	HLtime_1															
	2	Tdc															
	3	other_ch_1															
	4	dc															
	5	T															
	6																
	7	fault_pinstate															

Table 5. DCmDt Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW2	0	LHtime_2															
	1	HLtime_2															
	2	T_copy															
	3	center_time															
	4	DT															
	5	MPW															
	6																
	7																
SW3	0	LHtime_3															
	1	HLtime_3															
	2	L															
	3	other_ch_3															
	4	current															
	5	sync_presc_addr															
	6																
	7																
SW4	0	LHtime_4															
	1	HLtime_4															
	2	C															
	3	D															
	4																
	5																
	6																
	7																

Table 6. DCmDt parameter description

Parameter	Format	Description
Parameters written by CPU		
dc	16-bit fractional	duty-cycle ratio in the range <–1,1)
current	0 or 1	0 ... positive motor current 1 ... negative motor current
T	16-bit unsigned integer	PWM period in number of TCR1 TPU cycles
DT	16-bit unsigned integer	Dead-time in number of TCR1 TPU cycles
MPW	16-bit unsigned integer	Minimum pulse width in number of TCR1 TPU cycles. See **Performance** for details.
sync_presc_addr	8-bit unsigned integer	address of synchronization channel *prescaler* parameter: $X4, where X is synchronization channel number. $0 if no synchronization channel is used.
Parameters written by TPU		
fault_pinstate	0 or 1	If fault channel is used, state of fault pin: 0 ... low 1 ... high
Other parameters are just for TPU function inner use.		

Performance

Table 7. DCmDt State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	82	24
STOP	26	0
C10	6	1
C1	80	13
C20	6	2
C2	54	21
LH	2	1
HL	2	1

Execution times do not include the time slot transition time (TST = 10 or 14 IMB clocks)

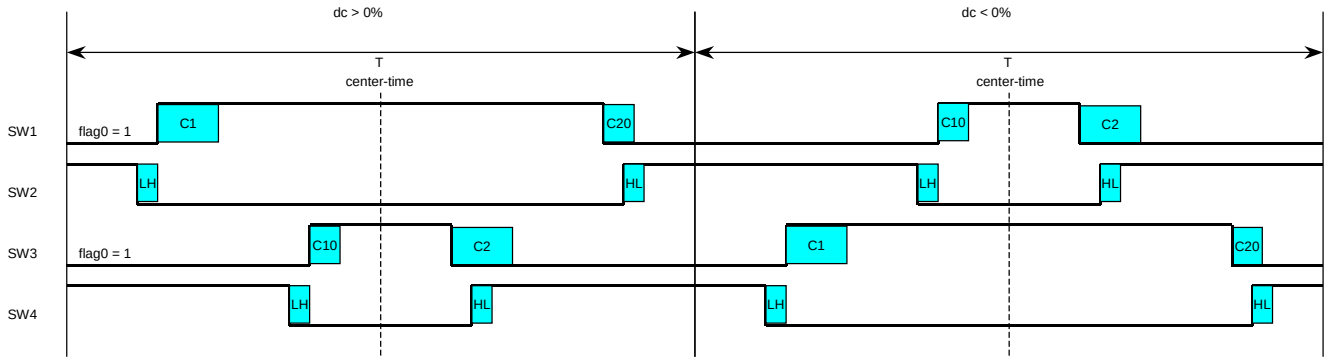

Figure 4. DCmDt timing

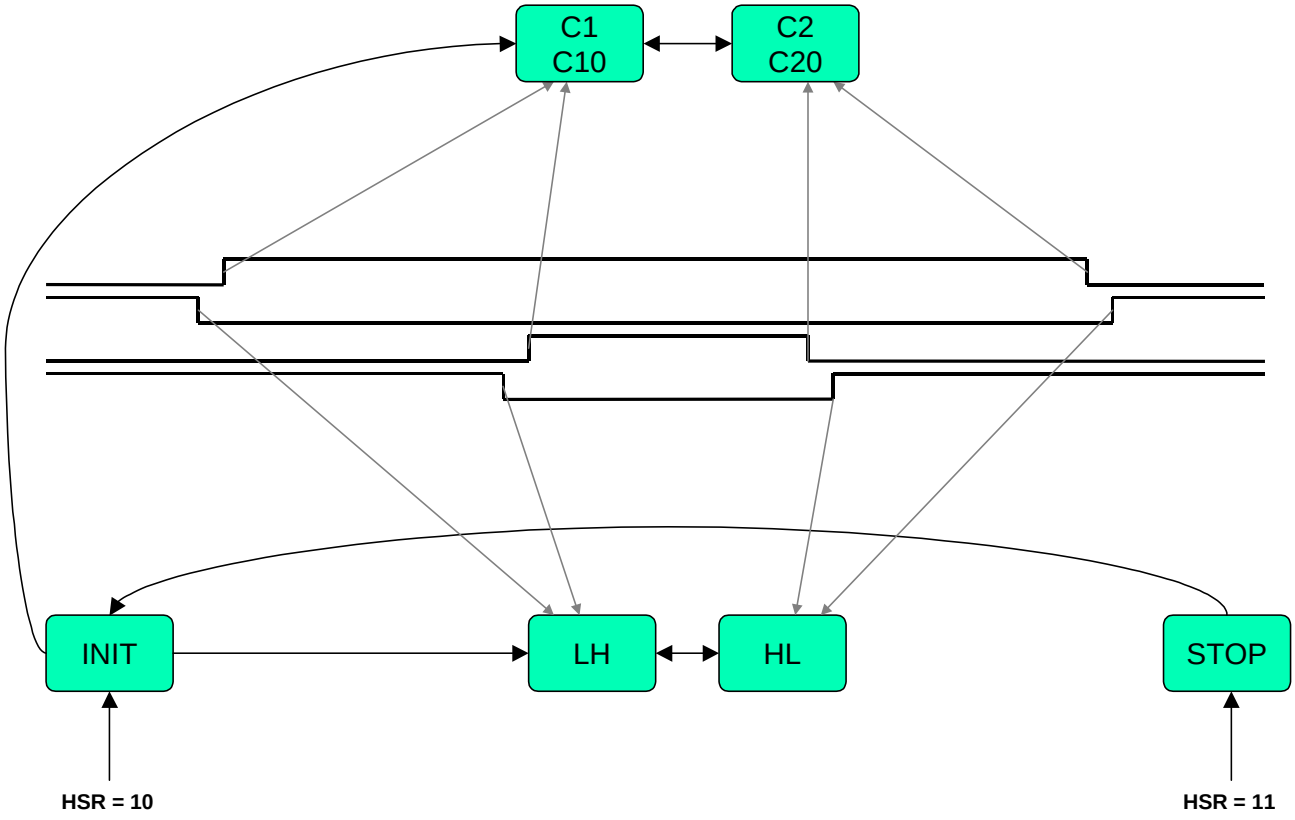

Figure 5. DCmDt state diagram

Minimum Pulse Width

The TPU cannot generate PWM signals with duty cycle ratios very close to 0% or 100%. This is the case when the *dc* value is close to 1 or –1. The minimum pulse width that the TPU can be guaranteed to generate correctly is determined by the TPU function itself and by the activity on the other channels. When the TPU function is requested to generate a narrower pulse a collision can occur. To prevent this, the parameter *MPW* (minimum pulse width) is introduced. The TPU function DCmDt limits the narrowest generated pulse widths to *MPW*. The CPU program should check the maximum absolute value of *dc* to prevent the limitation, or take into account the non-linear performance when *dc* moves towards the boundary values and the limitation is reached by the TPU. The maximum absolute value of *dc* should satisfy:

$$|dc| \leq 1 - \frac{2(MPW + 2DT)}{T}$$

The *MPW* is written by the CPU. The *MPW* depends on the whole TPU unit configuration, especially the lengths of the longest states of the other functions, and their prioroties, running on the same TPU and their priorities. The *MPW* has to be correctly calculated at the time of the whole TPU unit configuration.

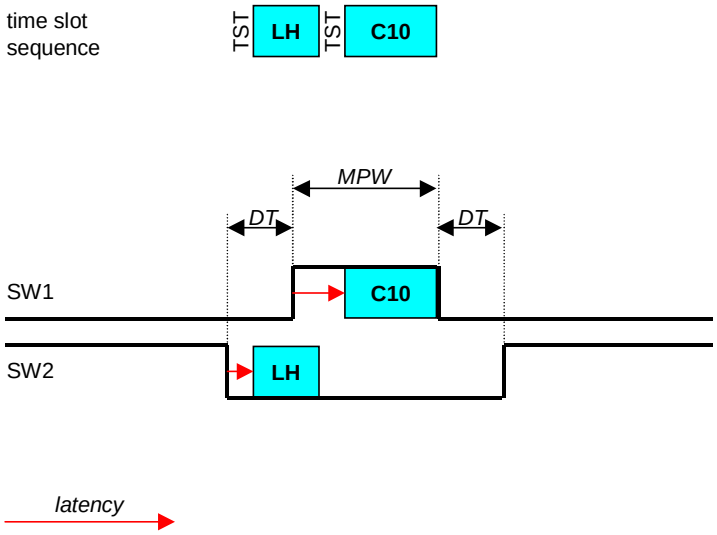

Figure 6. Worst case timing – case one

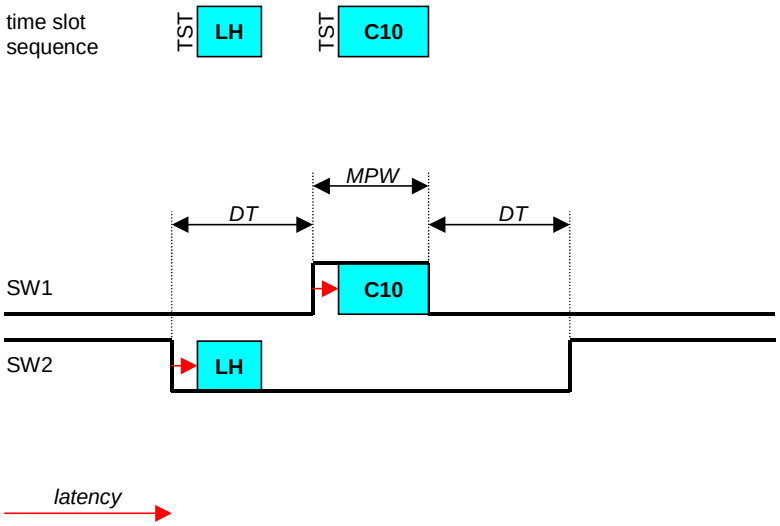

Figure 7. Worst case timing – case two

The minimum pulse width can be calculated according to **Figure 6** or **Figure 7**. These illustrate two possible worst cases of timing in the case when only DCmDt function is running on one TPU.

According to the **Figure 6** the *MPW* is 28 IMB clock cycles – *DT*. According to **Figure 7** the *MPW* is 16 IMB clock cycles. In summary the MPW parameter value is equal to 28 IMB clock cycles – *DT*, with a minimum value of at least 16 IMB clock cycles.

Note that the *MPW*, as well as the *DT*, are entered into the parameter RAM in TCR1 clock cycles rather that IMB clock cycles. It is recommended for the DCm2 function, to configure the TCR1 clock to its maximum speed, which is the IMB clock divided by 2. In this case the *MPW* = 14 – *DT*, with a minimum value of 8.

When other functions are running concurrently on the same TPU, the longest state of each function with its time-slot transition can increase the calculated *MPW* value. The DCmDt_fault function does not affect the *MPW*. The DCmDt_sync, if used, increase the *MPW* value by 22 (44 IMB clock cycles). The DCmDt_res, if used, increase the *MPW* value by 20 (40 IMB clock cycles).

If a value lower than the one calculated is assigned to the *MPW* parameter, the motion system can run with a higher motor voltage amplitude, but with a very low probability risk that the dead-time is not kept.

You can also use the Worst-Case Latency (WCL) that is automatically calculated by the MPC500_Quick_Start Graphical Configuration Tool. It can serve as a good approximation of *MPW*. The calculated WCL is always longer than the real-case is. Let the WCL be calculated after the configuration of the TPU channels and then find the longest WCL value within all the DCmDt PWM channels. Convert the number from IMB clock cycles to TCR1 clock cycles, to get the *MPW*.

Synchronization signal for DC Motor with Dead-Time Correction (DCmDt_sync)

The DCmDt_sync TPU function uses information obtained from DCmDt PWM functions, the actual PWM center times and the PWM periods. This allows a signal to be generated, that tracks the changes in the PWM period and is always synchronized with the PWM. The synchronization signal is a positive pulse generated repeatedly after the *prescaler* or *presc_copy* PWM periods (see next paragraph). The low to high transition of the pulse can be adjusted by a parameter, either negative or positive, to go before or after the PWM period center time of a number of TCR1 TPU cycles. The pulse width *pw* is another synchronization signal parameter.

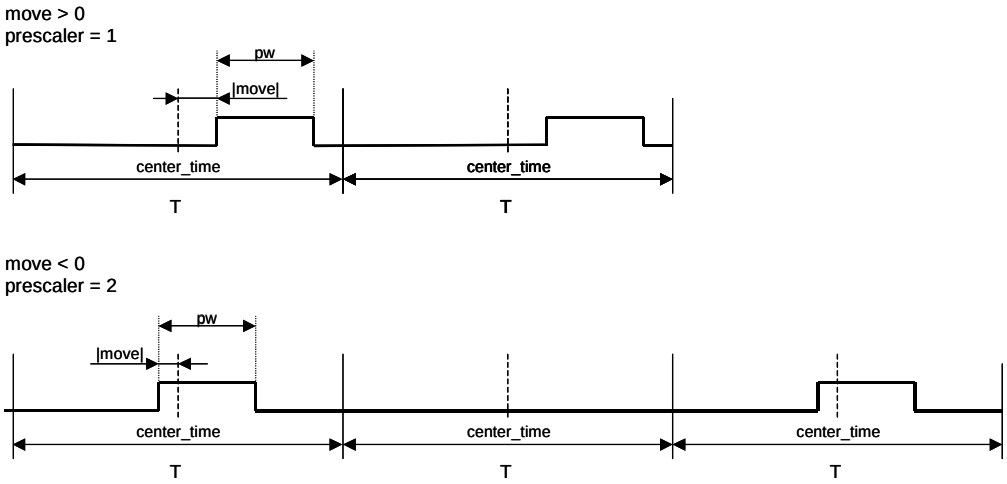

Figure 8. Synchronization signal adjustment examples

Synchronized Change of PWM Prescaler And Synchronization Signal Prescaler

The DCmDt_sync TPU function actually uses the *presc_copy* parameter instead of the *prescaler* parameter. The *prescaler* parameter holds the prescaler value that is copied to the *presc_copy* by the DCmDt_bottom function at the time of the PWM parameters reload. This ensures that new prescaler values for the PWM signals, as well as the synchronization signal, are applied at the same time. Write the synchronization signals *prescaler* parameter address to the *sync_presc_addr* parameter to enable this mechanism. Write 0 to disable it, and remember to set the synchronization signal *presc_copy* parameter instead of the *prescaler* parameter in this case.

Host Interface

Written By CPU

Written by both CPU and TPU

Written By TPU

Not Used

Table 8. DCmDt_sync Control Bits

Name	Options
3 2 1 0 Channel Function Select	DCmDt_sync function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
1 0 Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Not used
1 0 Host Sequence Bits (HSQ)	xx – Not used
0 Channel Interrupt Enable	0 – Channel Interrupt Disabled 1 – Channel Interrupt Enabled
0 Channel Interrupt Status	0 – Interrupt Not Asserted 1 – Interrupt Asserted

TPU function DCmDt_sync generates an interrupt after each low to high transition.

Table 9. DCmDt_sync Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Synchronization channel	0	move															
	1	pw															
	2	prescaler															
	3	presc_copy															
	4	time															
	5	dec															
	6	T_copy															
	7																

Table 10. DCmDt_sync parameter description

Parameter	Format	Description
Parameters written by CPU		
move	16-bit signed integer	The number of TCR1 TPU cycles to forego (negative) or come after (positive) the PWM period center time
pw	16-bit unsigned integer	Synchronization pulse width in number of TCR1 TPU cycles.
prescaler	16-bit unsigned integer	The number of PWM periods per synchronization pulse – use in case of synchronized prescalers change
presc_copy	16-bit unsigned integer	The number of PWM periods per synchronization pulse – use in case of asynchronized prescalers change
Parameters written by TPU		
Other parameters are just for TPU function inner use.		

Performance

There is one limitation. The absolute value of parameter *move* has to be less then a quarter of the PWM period *T*.

$$|move| < \frac{T}{4}$$

Table 11. DCmDt_sync State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	12	5
S1	12	6
S2	8	3
S3	16	7

NOTE: *Execution times do not include the time slot transition time (TST = 10 or 14 IMB clocks)*

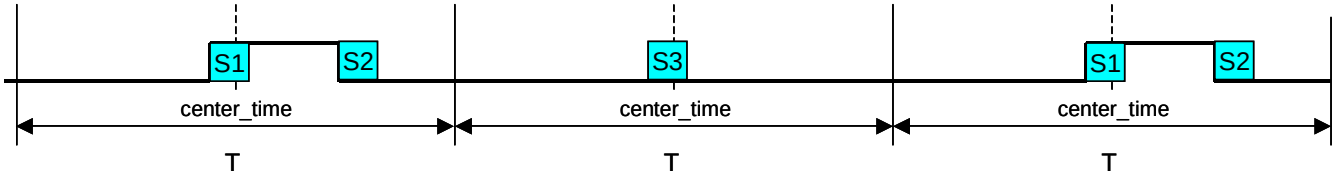

Figure 9. DCmDt_sync timing

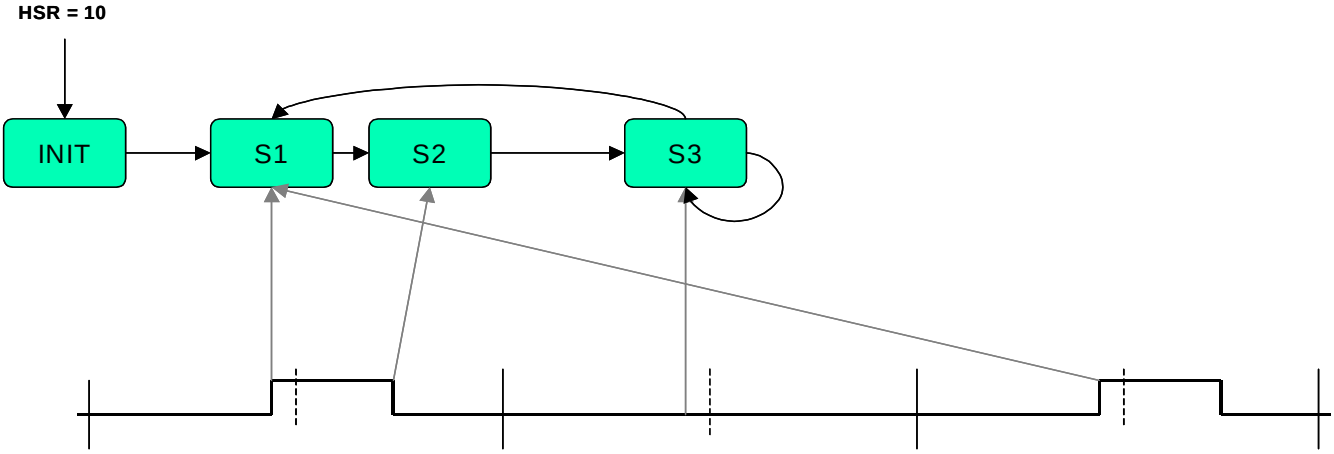

Figure 10. DCmDt_sync state diagram

Resolver Reference Signal for DC Motor with Dead-Time Correction (DCmDt_res)

The DCmDt_res TPU function uses information read from the DCmDt PWM functions, the actual PWM center times and the PWM periods. This allows a signal to be generated, which tracks the changes of the PWM period and is always synchronized with the PWM. The resolver reference signal is a 50% duty-cycle signal with a period equal to *prescaler* or synchronization channel *presc_copy* PWM periods (see next paragraph). The low to high transition of the pulse can be adjusted by a parameter, either negative or positive, to go before or after the PWM period center time of a number of TCR1 TPU cycles.

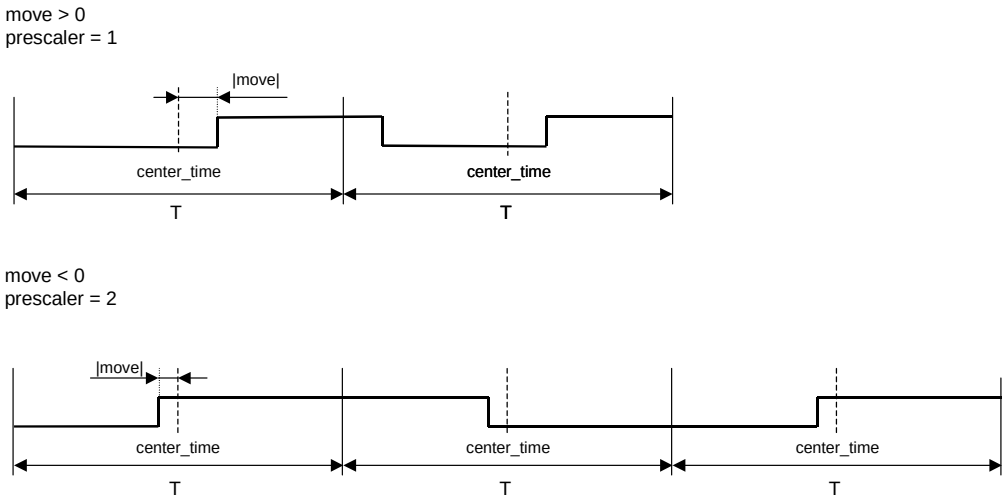

Figure 11. Resolver reference signal adjustment examples

Synchronized Change of PWM Prescaler And Resolver Reference Signals Prescaler

The DCmDt_res TPU function can inherit the Synchronization Signal prescaler that is synchronously changed with PWM prescaler. Write the synchronization signals *presc_copy* parameter address to the *presc_addr* parameter to enable this mechanism. Write 0 to disable it, and in this case set *prescaler* parameter to directly specify prescaler value.

Host Interface

Written By CPU

Written by both CPU and TPU

Written By TPU

Not Used

Table 12. DCmDt_res Control Bits

Name	Options
3 2 1 0 Channel Function Select	DCmDt_res function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
1 0 Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Not used
1 0 Host Sequence Bits (HSQ)	xx – Not used
0 Channel Interrupt Enable	x – Not used
0 Channel Interrupt Status	x – Not used

Table 13. DCmDt_res Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Resolver	0	move															
	1																
	2	presc_addr															
	3	prescaler															
	4	time															
	5	dec															
	6	T_copy															
	7																

Table 14. DCmDt_res parameter description

Parameter	Format	Description
Parameters written by CPU		
move	16-bit signed integer	The number of TCR1 TPU cycles to forego (negative) or come after (positive) the PWM period center time
presc_addr	16-bit unsigned integer	$00X6, where X is a number of Synchronization Signal channel, to inherit Sync. channel prescaler or $0000 to enable direct specification of prescaler value in prescaler parameter
prescaler	1, 2, 4, 6, 8, 10, 12, 14, ...	The number of PWM periods per synchronization pulse – use when apresc_addr = 0
Parameters written by TPU		
Other parameters are just for TPU function inner use.		

Performance

There is one limitation. The absolute value of parameter *move* has to be less than a quarter of the PWM period *T*.

$$|move| < \frac{T}{4}$$

Table 15. DCmDt_res State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	12	5
S1	26	9
S3	16	7

NOTE: *Execution times do not include the time slot transition time (TST = 10 or 14 IMB clocks)*

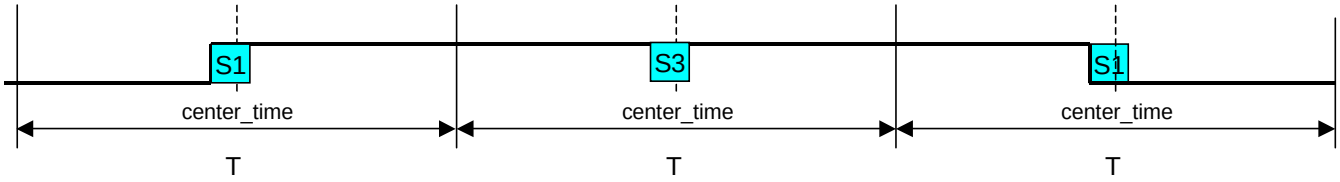

Figure 12. DCmDt_res timing

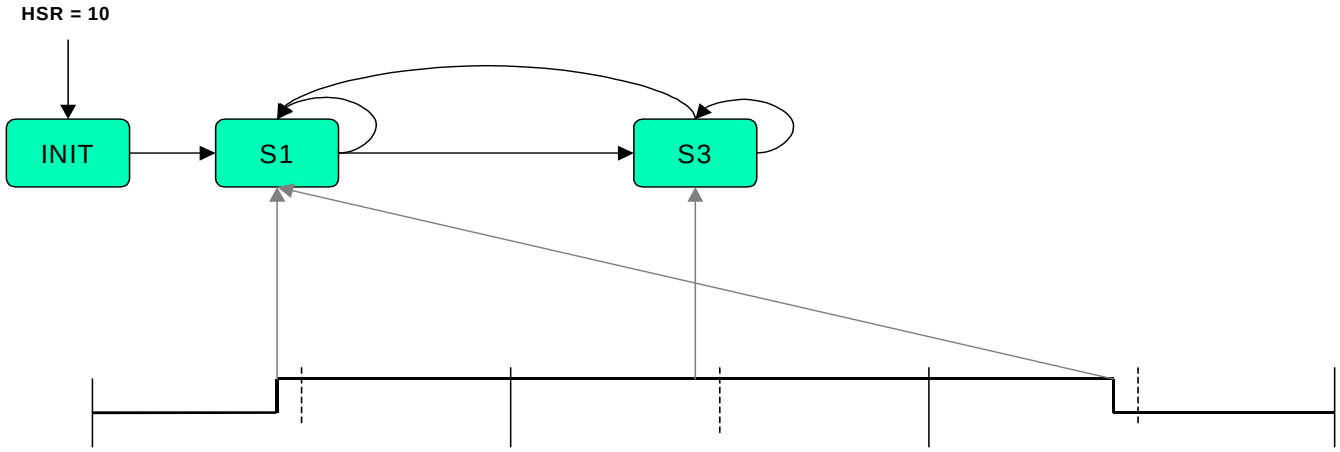

Figure 13. DCmDt_res state diagram

Fault Input for DC Motor with Dead-Time Correction (DCmDt_fault)

The DCmDt_fault is an input TPU function that monitors the pin, and if a high to low transition occurs, immediately sets all PWM channels low and cancels all further transitions on them. The PWM channels, as well as the synchronization and resolver reference signal channels (if used), have to be initialized again to start them running.

The function returns the actual pinstate as a value of 0 (low) or 1 (high) in the parameter *fault_pinstate*. The parameter is placed on the SW1 channel to keep the fault channel parameter space free.

Host Interface

Written By CPU

Written by both CPU and TPU

Written By TPU

Not Used

Table 16. DCmDt_fault Control Bits

Name	Options
3 2 1 0 Channel Function Select	DCmDt_fault function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
1 0 Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Not used
1 0 Host Sequence Bits (HSQ)	xx – Not used
0 Channel Interrupt Enable	0 – Channel Interrupt Disabled 1 – Channel Interrupt Enabled
0 Channel Interrupt Status	0 – Interrupt Not Asserted 1 – Interrupt Asserted

TPU function DCmDt_fault generates an interrupt when a high to low transition appears.

Table 17. DCmDt_fault Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fault input	0																
	1																
	2																
	3																
	4																
	5																
	6																
	7																

Table 18. DCmDt_fault parameter description

Parameter	Format	Description
Parameters written by TPU		
fault_pinstate	0 or 1	State of fault pin: 0 ... low 1 ... high

Performance

Table 19. DCmDt_fault State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	8	2
FAULT	32	1
NO_FAULT	4	1

NOTE: *Execution times do not include the time slot transition time (TST = 10 or 14 IMB clocks)*

Figure 14. DCmDt_fault timing

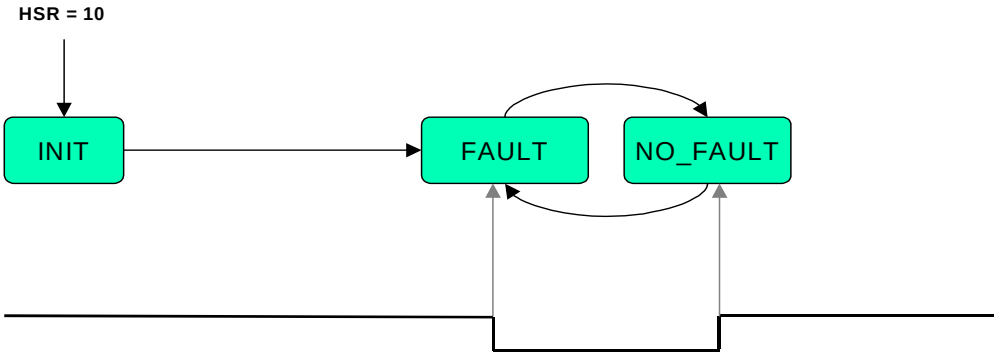

Figure 15. DCmDt_fault state diagram

[redacted]

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