

AN11513

BGU8M1 LTE LNA evaluation board

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Application note

Document information

Info	Content
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Abstract	This document explains the BGU8M1 LTE LNA evaluation board
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Contact information	For more information, please visit: http://www.nxp.com



Revision history

Rev	Date	Description
2	20160108	Updated with extra application information
1	20140423	First publication

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1. Introduction

NXP Semiconductors' BGU8M1 LTE LNA Evaluation Board is designed to evaluate the performance of the LTE LNA using:

- NXP Semiconductors' BGU8M1 LTE Low Noise Amplifier
- A matching inductor
- A decoupling capacitor

NXP Semiconductors' BGU8M1 is a low-noise amplifier for LTE receiver applications in a plastic, leadless 6 pin, extremely thin small outline SOT1232 at 1.1 x 0.7 x 0.37mm, 0.4mm pitch. The BGU8M1 features gain of 13 dB and a noise figure of 0.8 dB at a current consumption of 5 mA. Its superior linearity performance removes interference and noise from co-habitation cellular transmitters, while retaining sensitivity. The LNA components occupy a total area of approximately 4 mm².

In this document, the application diagram, board layout, bill of materials, and typical results are given, as well as some explanations on LTE related performance parameters like input third-order intercept point IIP3, gain compression and noise.

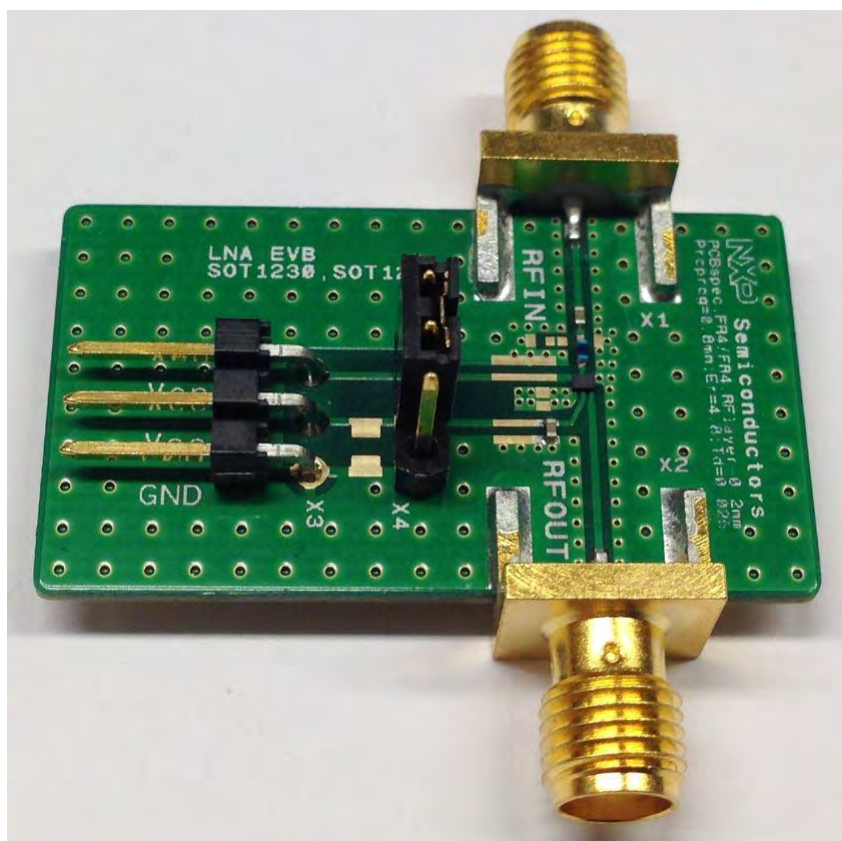


Fig 1. BGU8x1 LTE LNA evaluation board (used for BGU8L1, BGU8M1 and BGU8H1)

2. General description

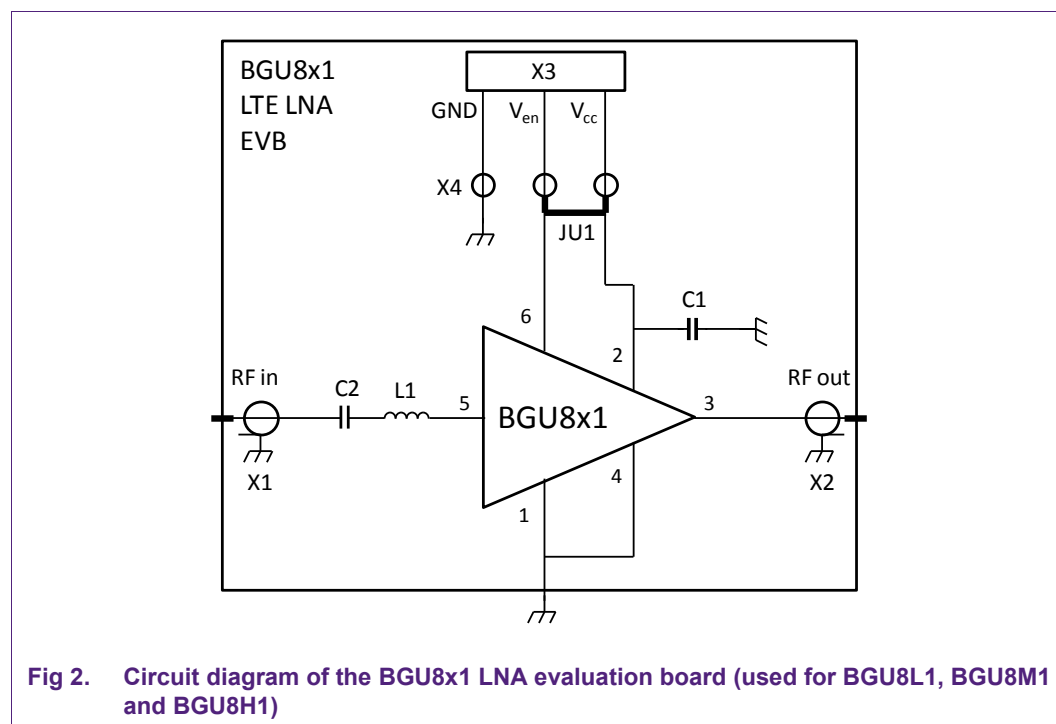
Modern cellular phones have multiple radio systems, so problems like co-habitation are quite common. Since the LTE diversity antenna needs to be placed far from the main antenna to ensure the efficiency of the channel, a low noise amplifier close to the antenna is used to compensate the track-losses (and SAW-filter losses when applicable) on the printed circuit board. A LTE receiver implemented in a mobile phone requires a low current consumption and low Noise Figure. All the different transmit signals that are active in smart phones and tablets can cause problems like inter-modulation and compression. Therefore also a high linearity is required.

3. BGU8M1 LTE LNA evaluation board

The BGU8M1LNA evaluation board simplifies the RF evaluation of the BGU8M1 LTE LNA applied in a LTE front-end, often used in mobile cell phones. The evaluation board enables testing of the device RF performance and requires no additional support circuitry. The board is fully assembled with the BGU8M1 including the input series inductor and decoupling capacitor. The board is supplied with two SMA connectors for input and output connection to RF test equipment. The BGU8M1 can operate from a 1.5 V to 3.1 V single supply and consumes typical 5 mA.

3.1 Application Circuit

The circuit diagram of the evaluation board is shown in Fig 2. With jumper JU1 the enable input can be connected either to Vcc or GND.



3.2 PCB Layout

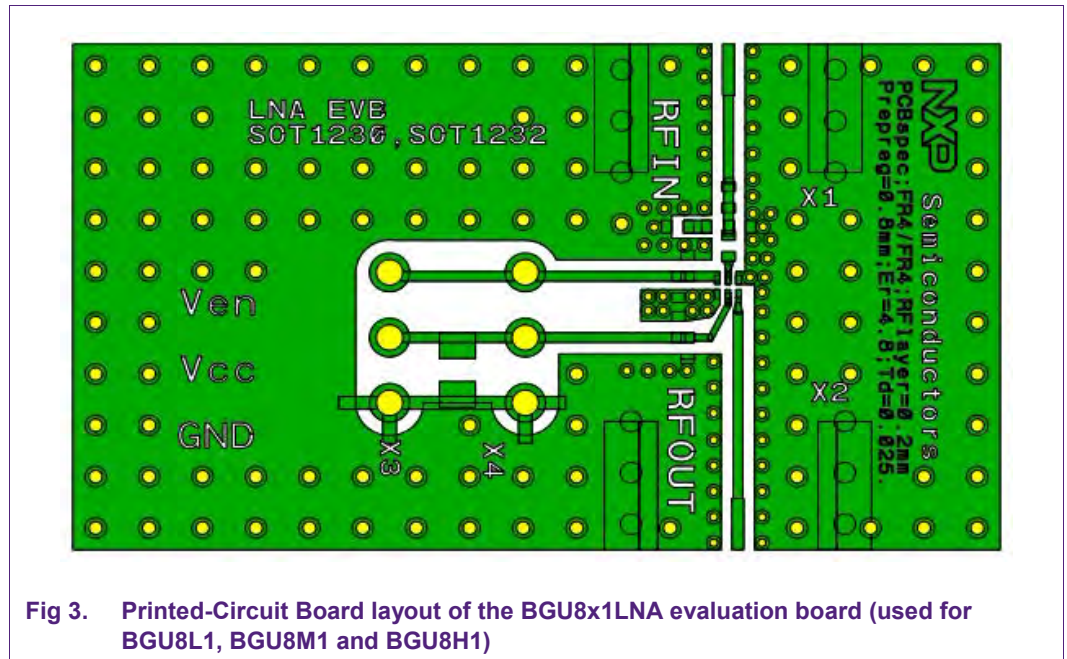


Fig 3. Printed-Circuit Board layout of the BGU8x1LNA evaluation board (used for BGU8L1, BGU8M1 and BGU8H1)

A good PCB layout is an essential part of an RF circuit design. The LNA evaluation board of the BGU8M1 can serve as a guideline for laying out a board using the BGU8M1. Use controlled impedance lines for all high frequency inputs and outputs. Bypass Vcc with decoupling capacitors, preferably located as close as possible to the device. For long bias lines it may be necessary to add decoupling capacitors along the line further away from the device. Proper grounding of the GND pins is also essential for good RF performance. Either connect the GND pins directly to the ground plane or through vias, or do both, which is recommended. The material that has been used for the evaluation board is FR4 using the stack shown in Fig 4.

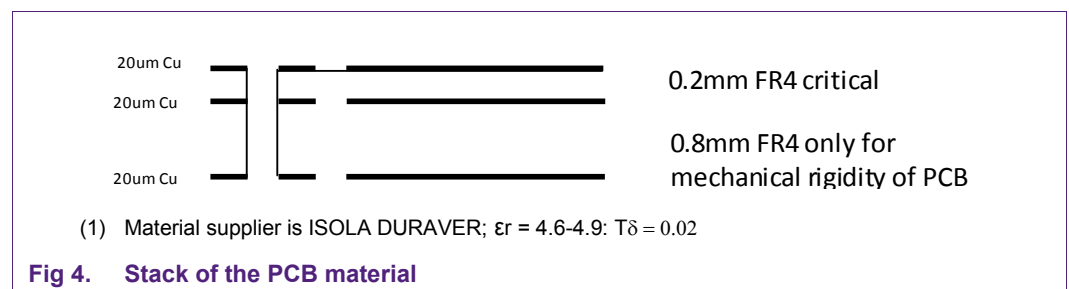


Fig 4. Stack of the PCB material

4. Bill of materials

Table 1. BOM of the BGU8M1 LTE LNA evaluation board

Designator	Description	Footprint	Value	Supplier Name/type	Comment
E	BGU8M1	1.1 x 0.7 x 0.37mm ³ , 0.4mm pitch		NXP	SOT1232
PCB		20 x 35mm		BGU8M1 LTE LNA EV Kit	
C1	Capacitor	0402	1nF	Murata GRM1555	Decoupling
C2	Capacitor	0402	1nF	Murata GRM1555	Decoupling
L1	Inductor	0402	3.3nH	Murata LQW15	Input matching
X1, X2	SMA RD connector	-	-	Johnson, End launch SMA 142-0701-841	RF input/ RF output
X3	DC header	-	-	Molex, PCB header, Right Angle, 1 row, 3 way 90121-0763	Bias connector
X4	JUMPER Stage	-	-	Molex, PCB header, Vertical, 1 row, 3 way 90120-0763	Connect Ven to Vcc or separate Ven voltage
JU1	JUMPER				

4.1 BGU8M1

NXP Semiconductors' BGU8M1 LTE low noise amplifier is designed for the LTE frequency band. The integrated biasing circuit is temperature stabilized, which keeps the current constant over temperature. It also enables the superior linearity performance of the BGU8M1. The BGU8M1 is also equipped with an enable function that allows it to be controlled via a logic signal. In disabled mode it consumes less than 1 μ A.

The output of the BGU8M1 is internally matched between 1805 MHz and 2200 MHz, whereas only one series inductor at the input is needed to achieve the best RF performance. The output is AC coupled via an integrated capacitor.

It requires only two external components to build a LTE LNA having the following advantages:

- Low noise
- System optimized gain
- High linearity under jamming
- 1.1 x 0.7 x 0.37, 0.4mm pitch: SOT1232
- Low current consumption
- Short power settling time

4.2 Series inductor

The evaluation board is supplied with Murata LQW15 series inductor of 3.3 nH. This is a wire wound type of inductor with high quality factor (Q) and low series resistance (Rs). This type of inductor is recommended in order to achieve the best noise performance.

High Q inductors from other suppliers can be used. If it is decided to use other low cost inductors with lower Q and higher Rs the noise performance will degrade.

5. Required Equipment

In order to measure the evaluation board the following is necessary:

- ✓ DC Power Supply op to 30 mA at 1.5 V to 3.1 V
- ✓ Two RF signal generators capable of generating RF signals at the LTE operating frequency of 1805 MHz to 2200 MHz.
- ✓ An RF spectrum analyzer that covers at least the operating frequency of 1805 MHz to 2200 MHz as well as a few of the harmonics. Up to 6 GHz should be sufficient.
“Optional” a version with the capability of measuring noise figure is convenient
- ✓ Amp meter to measure the supply current (optional)
- ✓ A network analyzer for measuring gain, return loss and reverse isolation
- ✓ Noise figure analyzer and noise source
- ✓ Directional coupler
- ✓ Proper RF cables

6. Connections and setup

The BGU8M1 LTE LNA evaluation board is fully assembled and tested (see Fig 5). Please follow the steps below for a step-by-step guide to operate the LNA evaluation board and testing the device functions.

1. Connect the DC power supply to the V_{cc} and GND terminals. Set the power supply to the desired supply voltage, between 1.5 V and 3.1 V, but never exceed 3.1 V as it might damage the BGU8M1.
2. Jumper JU1 is connected between the V_{cc} terminal of the evaluation board and the V_{en} pin of the BGU8M1.
3. Connect the RF signal generator and the spectrum analyzer to the RF input and the RF output of the evaluation board, respectively. Do not turn on the RF output of the signal generator yet, set it to approximately -40 dBm output power at center frequency of the wanted LTE-ban and\ set the spectrum analyzer at the same center frequency and a reference level of 0 dBm.
4. Turn on the DC power supply and it should read approximately 4..5 mA.
5. Enable the RF output of the generator: The spectrum analyzer displays a tone around -26 dBm.
6. Instead of using a signal generator and spectrum analyzer one can also use a network analyzer in order to measure gain as well as in- and output return loss, P1dB and IP3 (see Fig 6).
7. For noise figure evaluation, either a noise figure analyzer or a spectrum analyzer with noise option can be used. The use of a 5 dB noise source, like the Agilent 364B is recommended. When measuring the noise figure of the evaluation board, any kind of adaptors, cables etc between the noise source and the evaluation board should be minimized, since this affects the noise figure (see Fig 7).

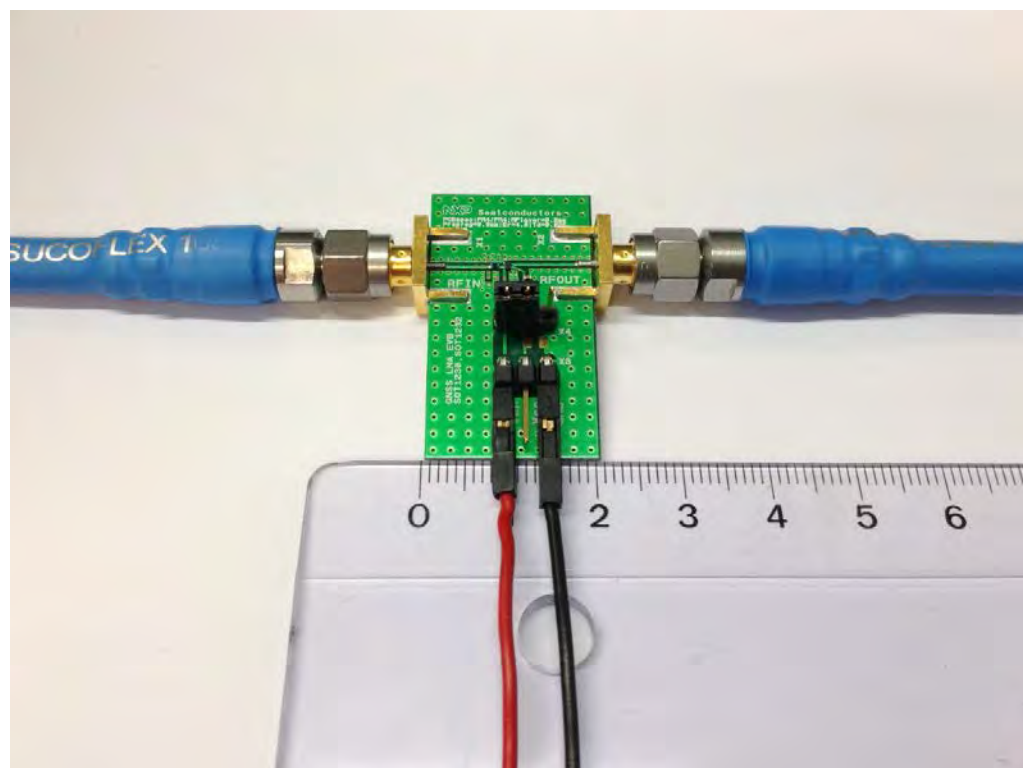


Fig 5. Evaluation board including its connections

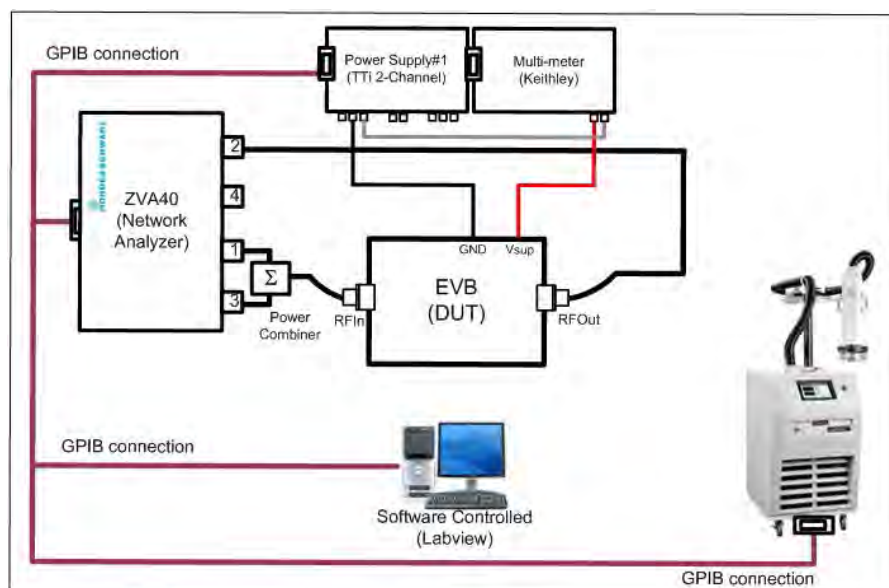


Fig 6. 2-Tone Setup for 50Ω LNA board tests (S-Parameters, P1dB and 2-Tone-tests)

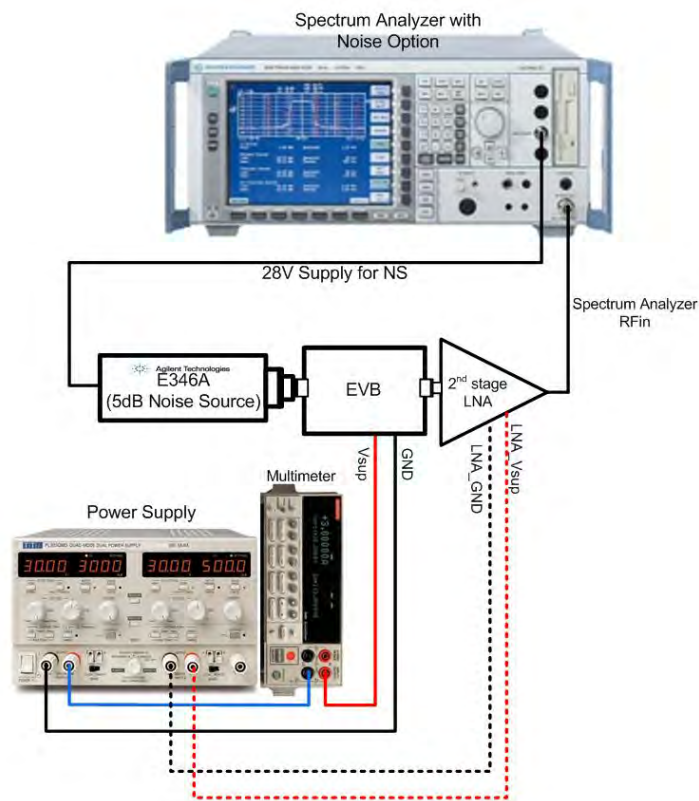


Fig 7. Setup diagram for 50Ω LNA-board NF-Measurements.

7. Evaluation Board Tests

7.1 S-Parameters

The measured S-Parameters and stability factor K are given in the figures below. For the measurements, a BGU8M1-LNA EVB is used ((see Fig 5). Measurements have been carried out using the setup shown in Fig 6.

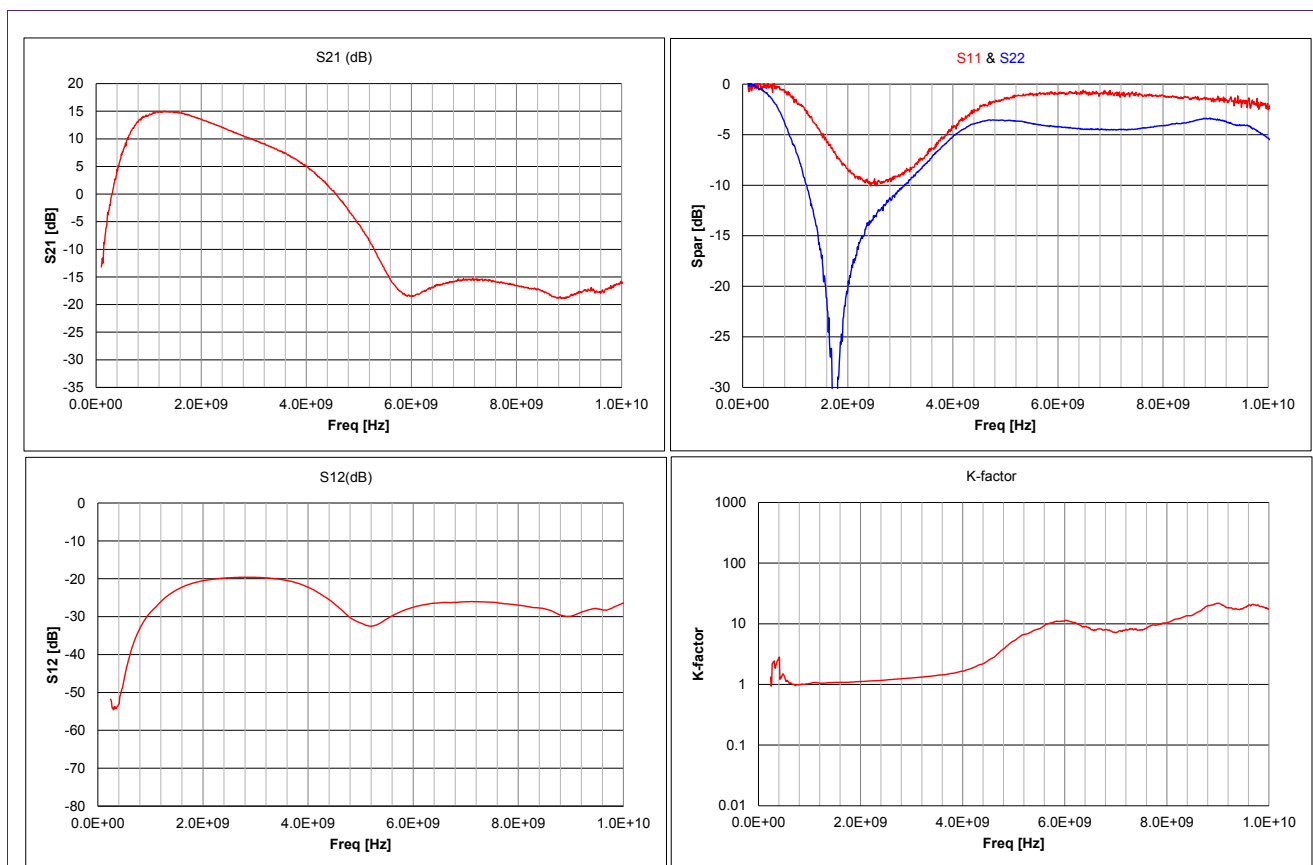


Fig 8. BGU8M1 S-Parameters (typical values). Vcc=2.8V, Pin=-45dBm.

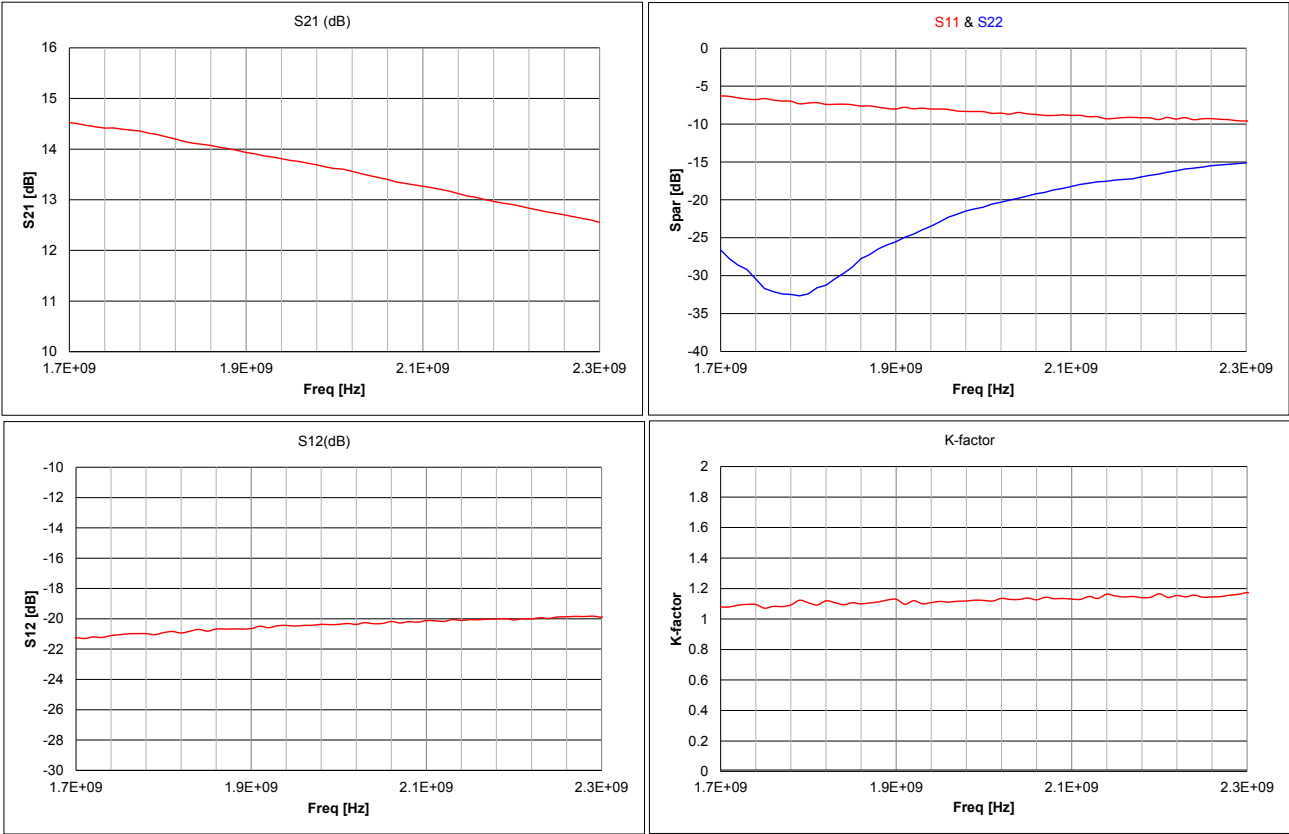


Fig 9. BGU8M1 S-Parameters (typical values). Vcc=2.8V, Pin=-45dBm (freq. range zoomed in).

7.2 1dB gain compression

Strong in-band cell phone TX jammers can cause linearity problems and result in third-order intermodulation products in the LTE frequency band. In this chapter the effects of these strong signals is shown. For the measurements, a BGU8M1-LNA EVB is used ((see Fig 5). Measurements have been carried out using the setup shown in Fig 6

The gain as function of input power of the DUT was measured between port RFin and RFout of the EVB at the LTE center frequencies.

The figures below show the gain compression curves at LNA-board.

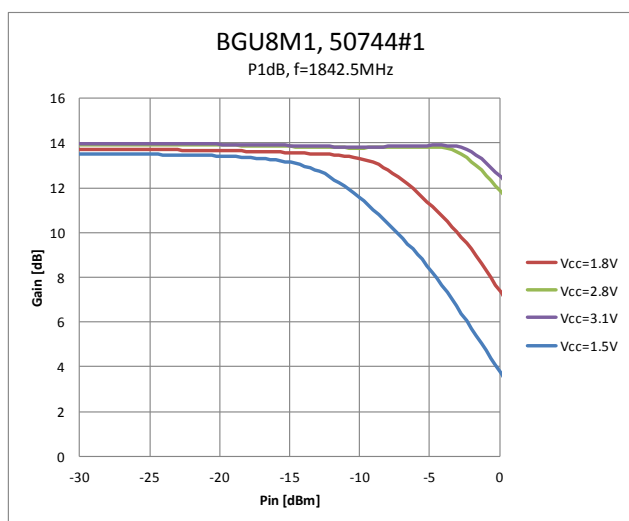


Fig 10. Gain versus inp. power, f=1842.5MHz (band 3)

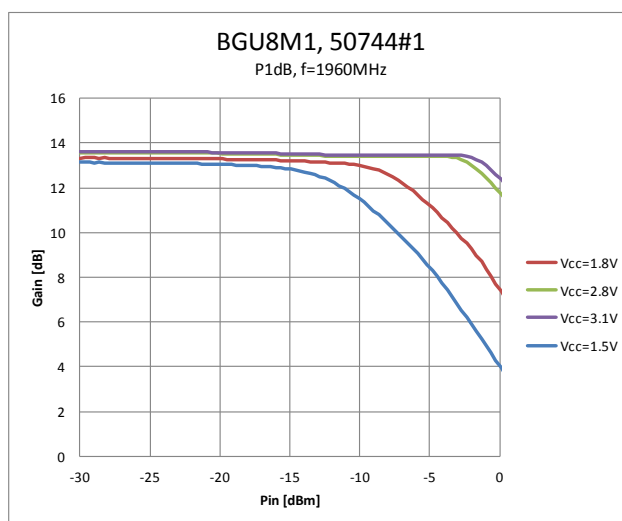


Fig 11. Gain versus input power, f=1960MHz (band 2)

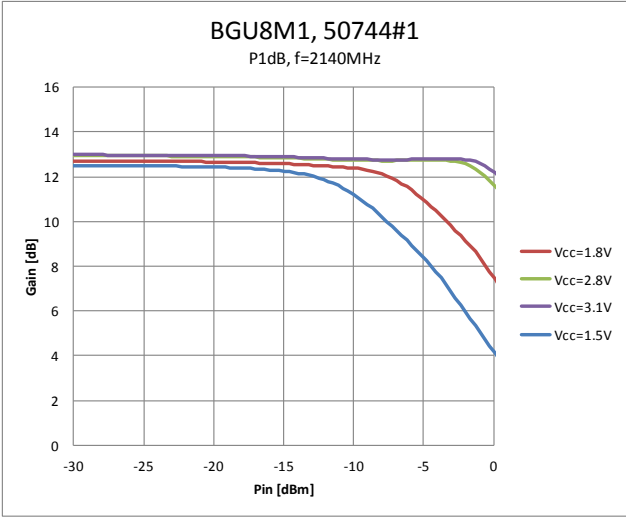


Fig 12. Gain versus input power, f=2140MHz (band 1)

7.3 2-Tone Test

The figures below show the spectra of the DUT caused by a 2-Tone input signal around the centre of the LTE-bands. For the measurements, a BGU8M1-LNA EVB is used ((see Fig 5). Measurements have been carried out using the setup shown in Fig 6.

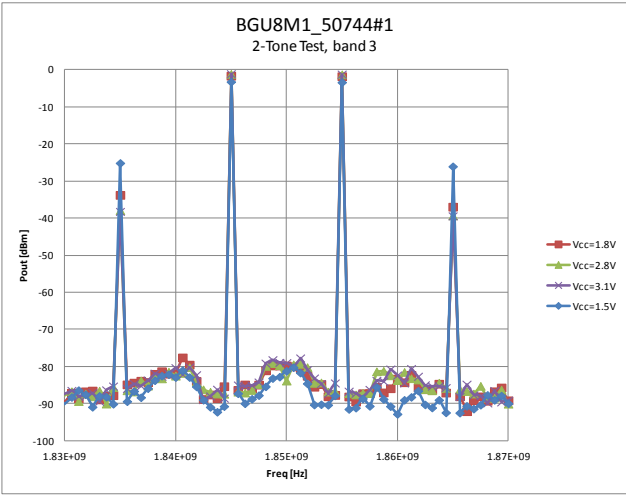


Fig 13. 2-Tone output spectrum, Pin=-15dBm, band 3

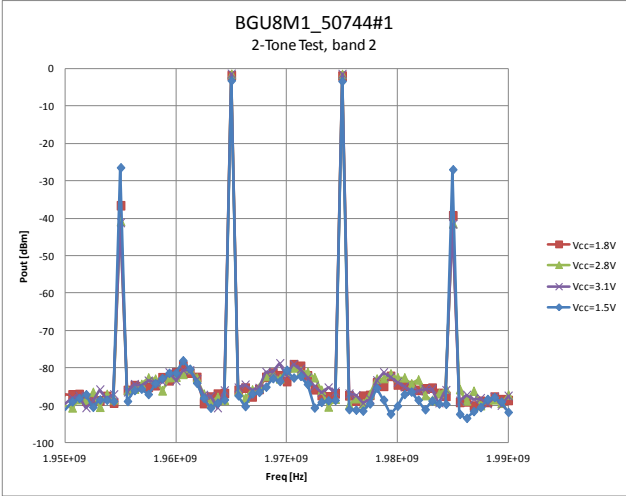


Fig 14. 2-Tone output spectrum, Pin=-15dBm, band 2

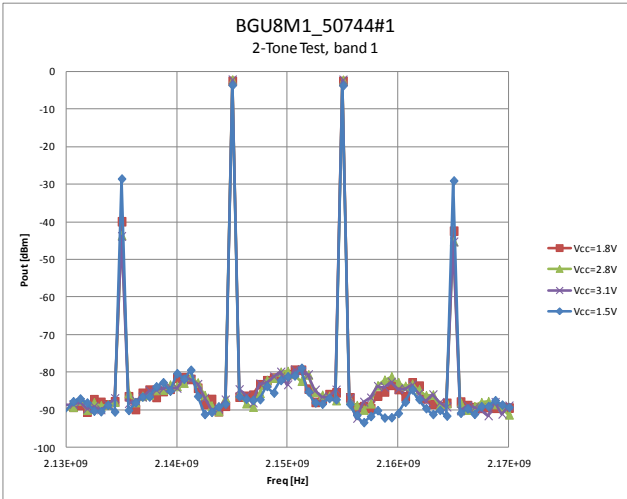


Fig 15. 2-Tone output spectrum, Pin=-15dBm, band 1

7.4 Enable Timing Test

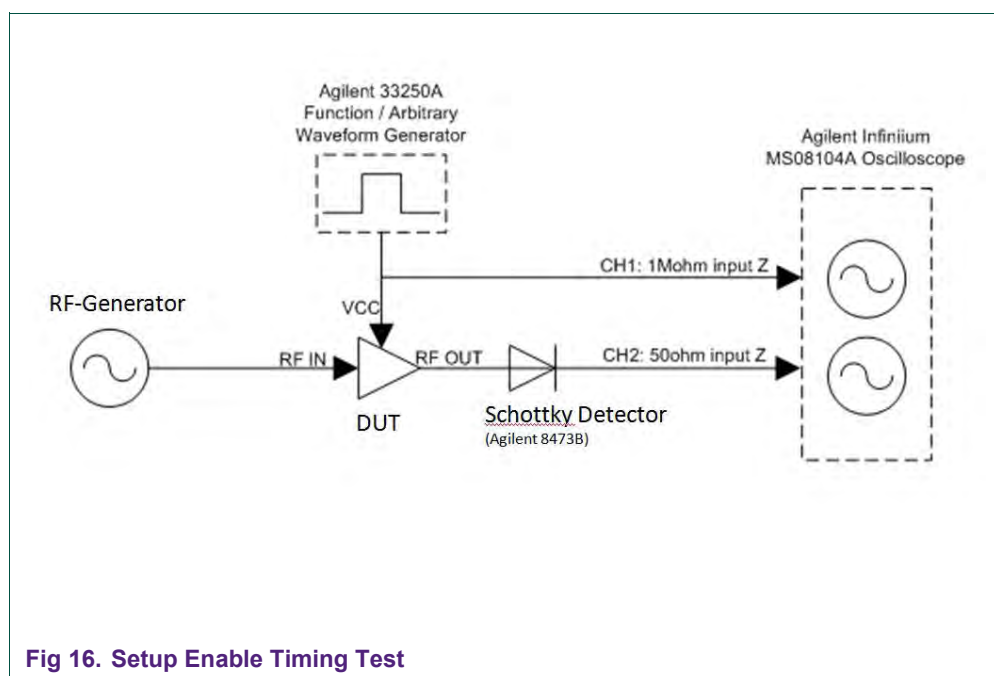
The following diagram shows the setup to test LNA Turn ON and Turn OFF time.

Set the waveform generator to square mode and the output amplitude at 3Vrms with high output impedance. The waveform generator has adequate output current to drive the LNA therefore no extra DC power supply is required which simplifies the test setup.

Set the RF signal generator output level to -20dBm between 1805 MHz and 2200 MHz and increase its level until the output DC on the oscilloscope is at 5mV on 1mV/division, the signal generator RF output level is approximately -3dBm.

It is very important to keep the cables as short as possible at input and output of the LNA so the propagation delay difference on cables between the two channels is minimized.

It is also critical to set the oscilloscope input impedance to 50ohm on channel 2 so the diode detector can discharge quickly to avoid a false result on the Turn OFF time testing.



The series capacitor will influence the Ton/Toff switching time. When the default value C2=1nF is used, Ton will approximately be 9us. By reducing C2 to 100pF, Ton is reduced to approximately 4μs (see Fig 17 and Fig 18).

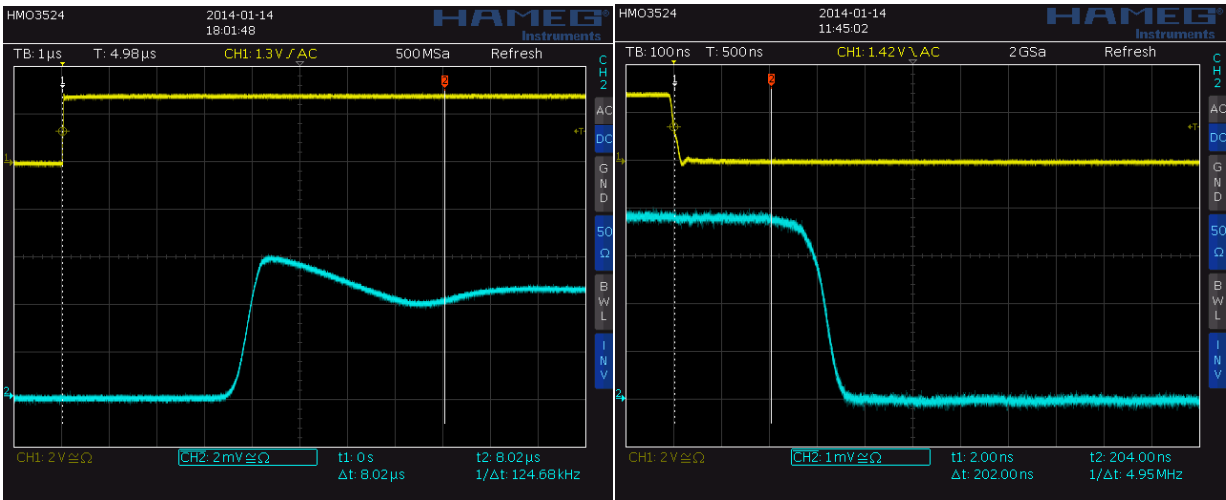


Fig 17. Results Enable Timing Test. Series capacitor C2=1nF. Ton~9µs (left) and Toff~200ns (right).

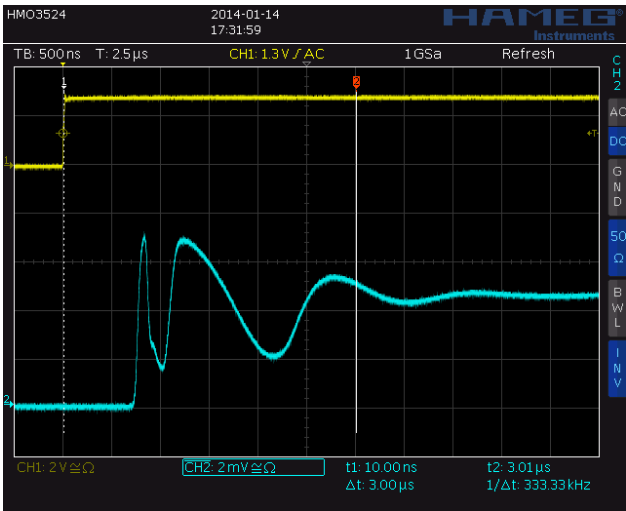


Fig 18. Results Enable Timing Test. Series capacitor C2=100pF. Ton~4µs (left).

8. Typical LNA evaluation board results

Table 2. Typical results measured on the evaluation Board.

Typical LNA evaluation board results Temp = 25 °C							
Parameter	Symbol	Freq. [MHz]					Notes
Supply Voltage	Vcc		1.5	1.8	2.8	3.1	V
Supply Current	Icc		4.6	4.7	5.0	5.3	mA
Noise Figure	NF	1840 1960 2140	0.90 0.90 1.00	0.90 0.90 1.00	0.90 0.90 1.00	0.90 0.90 1.00	dB [1]
Power Gain	Gp	1840 1960 2140	13.4 13.0 12.5	13.5 13.0 12.5	13.5 13.5 13.0	14.1 13.7 13.0	dB
Input Return Loss	RLin	1840 1960 2140	7 7 8	7 8 8	8 8 9	8 8 9	dB
Output Return Loss	RLout	1840 1960 2140	20 20 18	20 20 18	20 20 20	20 20 20	dB
Reverse Isolation	ISOrev	1840 1960 2140	21 20 20	20 20 20	20 20 20	21 20 20	dB
Input 1dB Gain Compression	Pi1dB	1840 1960 2140	-12.3 -11.6 -10.8	-8.0 -8.0 -7.0	-2.0 -2.0 -2.0	-0.8 -0.4 0.4	dBm
Output 1dB Gain Compression	Po1dB	1840 1960 2140	0.1 0.4 0.7	4.5 4.0 4.5	10.5 10.5 10.0	12.3 12.4 12.4	dBm
Input third order intercept point	IIP3	1840 1960 2140	-3.1 -2.7 -1.9	0.0 1.0 2.0	4.0 5.0 6.0	4.0 5.0 6.2	dBm [2]
Output third order intercept point	OIP3	1840 1960 2140	10.3 10.3 10.6	13.5 14.0 14.5	17.5 18.5 19.0	18.1 18.7 19.2	dBm [2]
Power settling time	Ton		4	4	4	4	µs
	Toff		1	1	1	1	µs

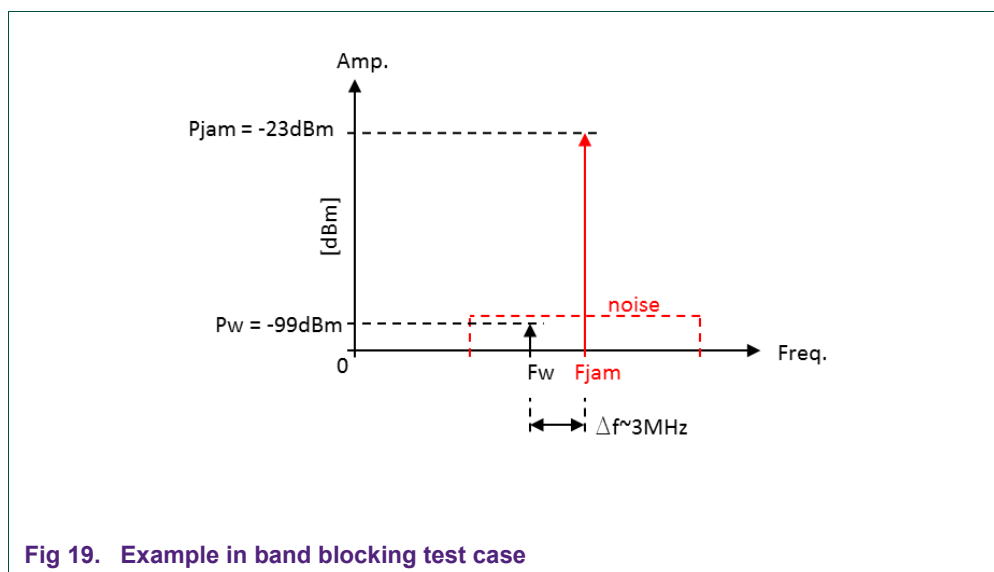
[1] Including PCB losses

[2] $f = f_{\text{center_band}}$; $\Delta f = 10\text{MHz}$

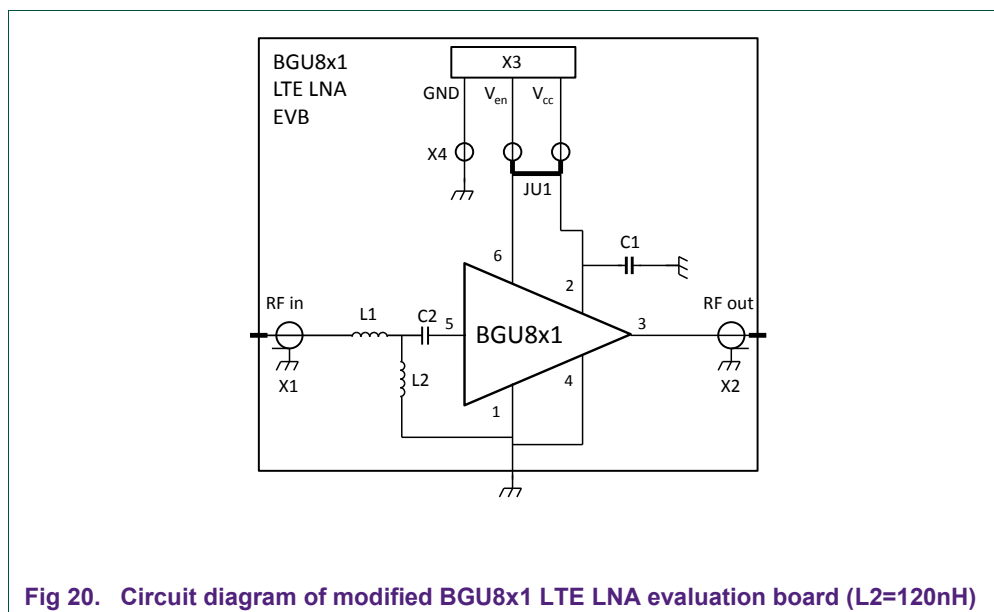
$\text{Pin}_{f_1} = \text{Pin}_{f_2} = -15\text{ dBm}$

9. Improved in band blocking performance modification

In some cases a strong in-band jamming signal is present, reducing the sensitivity. This in band blocking test case is illustrated below in Fig 19. A jamming signal causes an increase of the noise-floor closely around the jamming frequency, which reduces the sensitivity for a wanted signal overlapping with the noise band.



A solution is to make a low impedance path for low frequencies at the input of the LNA. This can be done by an additional shunt inductor L2 with a high value, as shown in the circuit of Fig 20 and board detail in Fig 21 (L1 and C2 have been swapped compared with Fig 2 to avoid a DC-path between RFin and GND). For L2 a Murata LQW15 wire wound inductor with a value of 120nH is used.



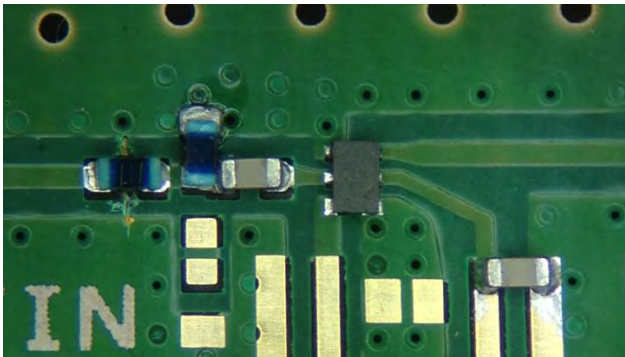
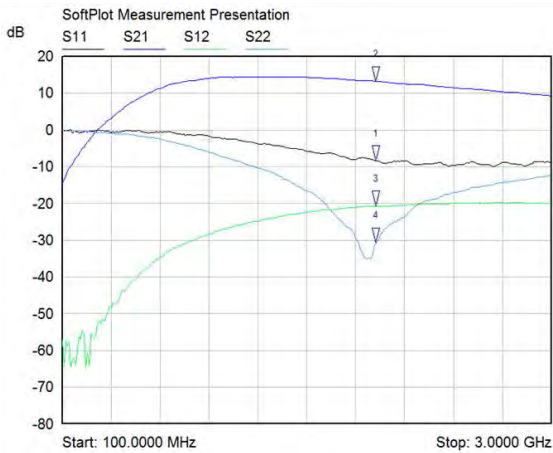


Fig 21. Detail of modified BGU8x1 LTE LNA evaluation board

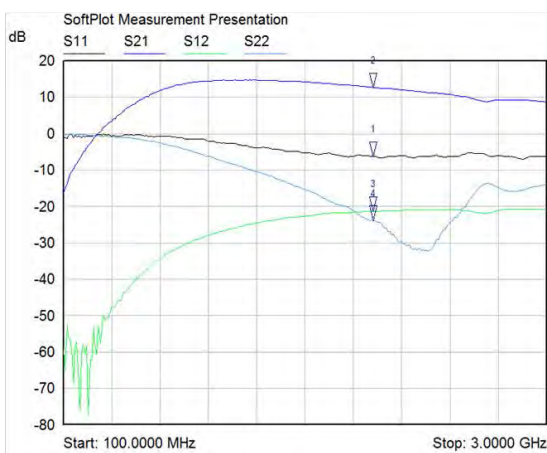
The measured performance is given in Fig 22 and Table 3. The Gain is reduced by approx. 0.5dB and the NF is increased with 0.1dB.

EVB #30, Vcc=2.8V, Default match.



Mkr	Trace	X-Axis	Value	Notes
1	S11	1.9600 GHz	-8.32 dB	
2	S21	1.9600 GHz	13.22 dB	
3	S12	1.9600 GHz	-20.73 dB	
4	S22	1.9600 GHz	-30.70 dB	

EVB #30, Vcc=2.8V, Modified input.



Mkr	Trace	X-Axis	Value	Notes
1	S11	1.9600 GHz	-6.25 dB	
2	S21	1.9600 GHz	12.74 dB	
3	S12	1.9600 GHz	-21.30 dB	
4	S22	1.9600 GHz	-23.76 dB	

Fig 22. Measured performance modified BGU8x1 LTE LNA evaluation board

Table 3. Typical results measured on the modified evaluation Board.

Typical LNA evaluation board results										
Temp [°C]	25	BGU8M1_95214								
P_Spar [dBm]	-45	3 EVB's								
Parameter		Symbol	Default typ	L2=120nH typ	Delta typ	Default typ	L2=120nH typ	Delta typ	Unit	Notes
		Freq. [MHz]								
Supply Voltage		Vcc	1.80V	1.80V	1.80V	2.80V	2.80V	2.80V	V	
Noise Figure	1840	NF							dB	
	1960		0.83	0.93	0.11	0.78	0.90	0.12		
	2140									
Power Gain	1840	Gp	13.2	12.8	-0.5	13.6	13.1	-0.5	dB	
	1960		12.9	12.3	-0.6	13.3	12.7	-0.6		
	2140		12.2	11.6	-0.6	12.6	11.9	-0.7		
Input Return Loss	1840	RLin	7.5	5.8	-1.7	7.9	6.1	-1.8	dB	
	1960		7.8	5.8	-2.0	8.2	6.1	-2.2		
	2140		8.0	5.6	-2.4	8.6	5.9	-2.7		
Output Return Loss	1840	RLout	28.7	21.0	-7.7	36.6	21.1	-15.5	dB	
	1960		32.0	24.2	-7.9	28.8	23.8	-5.1		
	2140		24.2	32.2	7.9	21.9	30.3	8.5		
Reverse Isolation	1840	ISOrev	21.1	21.6	0.5	21.0	21.6	0.6	dB	
	1960		20.7	21.3	0.6	20.6	21.3	0.7		
	2140		20.4	21.1	0.7	20.3	21.1	0.8		
Input 1dB Gain Compression	1840	Pi1dB	-7.3	-6.9	0.4	-1.3	-0.9	0.4	dBm	
	1960		-6.7	-6.4	0.4	-0.8	-0.4	0.4		
	2140		-5.9	-5.5	0.4	0.0	0.5	0.5		
Output 1dB Gain Compression	1840	Po1dB	5.0	4.8	-0.2	11.3	11.2	-0.1	dBm	
	1960		5.3	4.9	-0.3	11.5	11.2	-0.2		
	2140		5.4	5.1	-0.3	11.6	11.4	-0.2		
Input third order intercept point (average lsb&usb)	1840	IIP3	0.7	1.0	0.3	1.9	1.7	-0.2	dBm	
	1960		2.0	2.4	0.4	3.0	3.5	0.5		
	2140		2.9	3.4	0.5	3.7	4.3	0.7		
Output third order intercept point (average lsb&usb)	1840	OIP3	14.2	13.9	-0.2	15.6	15.0	-0.7	dBm	
	1960		15.2	15.1	-0.1	16.4	16.5	0.1		
	2140		15.2	15.2	-0.1	16.3	16.5	0.2		

Note: Noise Figure is including PCB losses.

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